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ADVANCED MATERIALS

French Firm Develops New Friction Composite

89AN0304 Paris FRENCH TECHNOLOGY SURVEY in English Jul-Aug 89 p 15

[Article: "Composite Friction Material"]

[Text] The composite material TS-811, developed by the Research Center in Mechanical Engineering, Hydraulics, and Friction and exploited by its subsidiary Techniques Surfaces, was intended to counteract the poor mechanical strength and wear resistance of polymers and the likelihood of destruction once forces are no longer centered on the load-bearing zone (PTFE or polyacetate impregnations on porous bronze on a metal sheet).

The TS-811 composite has the following advantages:

remarkable wear resistance at the maximum of what can be expected from polymer materials. For this reason it is suitable not only in operational situations at low load and high speed but also where there is friction at high load and low speed;

coefficients of friction comparable to those of materials supposed to have the best in "antifriction" properties;

zero sensitivity to edge forces owing to their very high accommodative power;

low sensitivity to thermal effects owing to its good thermal conductivity, its low coefficient of expansions and, finally, its good mechanical properties at higher temperatures;

excellent performance in the case of friction in acquiescent environments;

a production cost entirely comparable with that of widely available friction materials, such as strip bearings with PTFE impregnated sintered bronze, sintered iron bearings, or those with sintered bronze impregnated with oil.

The field of application of this material is enormous. As examples one may mention slides, swivels, piston rings, bearings, pistons, washers, dynamic seal seats, and so on.

AEROSPACE, CIVIL AVIATION

Chairman of France's GIFAS Delivers Aerospace Report

89AN0297 Paris LE BULLETIN DU GIFAS in English No 1492, 13 Jul 89 pp 1-2

[Report by Jacques-Andre Larpent, chairman of the French Aeronautics and Space Industries Group (GIFAS), to the GIFAS General Assembly on 6 July 1989]

[Text] The 38th International Air and Space Show held at Le Bourget from 8 to 18 June was an unprecedented success. The Soviet Union was well represented at this show, and one of its major attractions was a flight demonstration of the space shuttle Buran, carried by the Antonov 225. The show also provided an opportunity:

- for evaluating progress made in all branches: airframes, power plants, equipment, systems and space;
- for displaying French and other products to professional visitors from numerous countries and to a vast general public;
- favoring profitable contacts between customers and suppliers. The show was even the theater where various contracts were concluded.

The financial report of the past year shows a marked improvement over 1987. Our industry remains second in the Western world, after the United States, with a turnover of 83.4 billion francs, of which 49.4 billion was accounted for through exports, and [there are] 120.5 billion francs worth of orders pending. France shares this leading position with Britain. It is our industry that has obtained the most positive balance of payments (Fr 34 billion) of all French commercial industries.

The strong growth of the civil aeronautical market noted during the past few years accelerated in 1988 to such an extent that civil orders now exceed 51 percent.

Nevertheless, these excellent results and the even better results expected for 1989 must not hide from us the uncertainties of the future, subject to fluctuations in the geopolitical scene to which the aerospace industries of all countries are particularly sensitive.

Consequently, we must adhere to our basic goals:

- maintaining our technological and production capacity, so that our industry remains capable of executing national programs alone while participating in cooperation programs, either as industrial leader or full-fledged partner;
- maintaining our export capacity, indispensable for keeping up our need for highly qualified workers, at mother firms level [as published] or within the ranks of our suppliers and subcontractees, a condition for maintaining a positive and significant balance of payments.

These goals can only be attained at the price of continued efforts by the profession to expand existing military and civil sales networks and by marketing state-of-the-art competitive new or derived products in all branches (airframes, engines, equipment, space). This implies heavy investments in research and development and the establishment of funding power.

Our industry is preparing for the future by further development in many programs and by launching new programs (essentially, ACT/ACM, Airbus A330/A340 and A321, ATR 72, ATR-AMD Petrel, ATL 2, HAP/HAC, NH 90, the engines M88, CFM 56-5C-1, GE 36,

MCV 99, Vulcain, the Orchidee and Brevel systems, the missiles Eryx, ANS, Aster, Saam, Milas, Mistral, Apache, Mica, and, in the space field, the Ariane 5, Columbus, Hermes and Helios).

Many of these programs are handled on a cooperation basis in order to obtain a substantial reduction in development costs, which, in recent years, have grown considerably, and to increase production batches.

This seemingly favorable growth situation should not prevent us from being prudent and realistic.

In the civil field, many orders would seem to be primarily speculative in nature, and the situation might easily fall apart in the event of a change in the general economical scene.

In the military field, there is, on the one hand, a significant potential market for replacing fighter aircraft of the sixties, but on the other hand, a danger of a slump because of a gearing-down of the national defense effort combined with a general trend to disarmament. With the Europe of 1993 close on the horizon, there are still problems connected with a common armament market favoring European industry.

Within this context, the organizations of the leading European countries differ. While Britain and the Federal Republic of Germany have decided to denationalize their industries and create highly powerful groups, the French aeronautical and space industry is 90 percent nationalized and remains relatively scattered.

For France, there is no miracle solution. The basic task remains to work together with the competent authorities to devise an overall economic policy and to apply it with determination, particularly for:

- financing studies and the development of products;
- supporting our export effort;
- opening the European armament market.

It is through the combined efforts of the official French services and the profession itself that the French aerospace industry will be able to make an important contribution to the independence and expansion of our country throughout the world and contribute significantly to the national economy and a healthy exchange balance with stability and expansion of employment.

Ceramic Materials for Hermes Spacecraft Being Tested

36980253 Madrid YA in Spanish 24 May 89 p 23
24 May 89 p 23

[Article: "Spacecraft Hulls: Between Ice and Fire"]

[Excerpt] [Passage omitted]

Protective 'Shield'

The evaporators can be activated either in the atmospheric phase of the flight or in orbit, and control the ranging of the heat load. The water can be used at altitudes in excess of 40 kilometers; to cool the ship at lower altitudes, the ammonia evaporators are activated.

There is also the problem of protection from the extremely high temperatures (up to 1,400 degrees) generated during reentry into the atmosphere. A heat shield for the Hermes is being tested at Almeria, which is intended to shield the zones of the hull most exposed to atmospheric heating. It consists of a ceramic coating and an insulating layer designated by the symbol IMI [identified by source as "Internal Insulating Screen"], interposed between the plates that form the ship's external shield and its structure.

The IMI consists of several layers of metallic materials: Molybdenum and platinum for the outermost layers, nickel for the intermediate layers, and aluminum for the innermost layers, intermixed with a layer of quartz and aluminum felt. Each level of the coating will have a thickness of 5 to 15 microns, with total thickness of the coating reaching 10 cm.

Hermes Project in Almeria

Since the end of last year, at the CIEMAT [Center for Energy, Environmental, and Technological Research Center] Renewable Energies Institute's PSA [Almeria Solar Plant], the thermomechanical properties of two ceramic materials have been being tested: Carbon-carbon and carbon-silicon carbide, which will protect the Hermes shuttle on its first flight, targeted for 1998.

In the opinion of the technicians at Almeria, carbon-silicon carbide fiber, because of its exceptional heat-resistant properties, offers advantages over the carbon-carbon fiber that forms the heat shield. Initial tests to determine the thermal cycles of the two materials were made on a mock-up of the Hermes shuttle, at extremely high simulated temperatures in a concrete tower 82 meters high, within which the test piece was placed. Behind it are the measuring equipment and setups that sense the tiniest thermal variations in the test piece.

BIOTECHNOLOGY

France Promoting Solar Synthesis Technology

89AN0303 Paris FRENCH TECHNOLOGY SURVEY in English Jul-Aug 89 p 13

[Article: "Solar Synthesis: A New Bio-Industry"]

[Text] Under an agreement concluded with the Atomic Energy Commission (CEA), USSI Ingenierie took over in January 1989 the promotion and marketing of the solar synthesis technologies developed at the Cadarache (Bouches du Rhone) Nuclear Research Center.

The laboratories and pilot solar reactors managed by USSI Ingenierie are used for the controlled culture of different species of microalgae and the extraction of high value-added molecules obtained by photosynthesis. The

first products targeted concern biomass, natural pigments, vitamins, polyunsaturated fatty acids and biological antioxidants, produced specifically by the micro-algae.

The current yields are on the order of 60 tonnes of dry biomass per sunlit hectare per year. The molecules of commercial interest, the concentrations of which are optimised by selection of strains and strict control of the specific culture parameters, can reach 5-10 percent of the biomass.

The metabolism of the micro-algae is orientated to the accumulation or excretion of certain molecules by varying carbonation, deoxygenation, the composition of the inorganic medium, and the rates of dilution. Techniques of harvesting, extraction and purification developed for each type of molecule place these products of natural origin in competition with chemical synthesis. This process already appears more economical for those molecules requiring a number of stages for syntheses.

It should be noted that USSI Ingenierie can offer a whole range of services covering knowledge and know-how acquired in solar synthesis:

- technical and economic feasibility studies;
- selection of strains;
- laboratory optimisation of media and culture parameters;
- development of techniques of harvesting, extracting and purifying molecules.

COMPUTERS

ESSI Software Project Introduced

89AN0299 Paris FRENCH TECHNOLOGY SURVEY in English Jul-Aug 89 p 1

[Article: "ESSI: Research Programme for Improving Software Productivity"]

[Text] Having decided to meet the Japanese and American challenge in the semiconductor field with JESSI (Joint European Submicron Silicon Initiative), Europe is now preparing to do the same in software with ESSI (European Systems and Software Initiative). This project, which aims to improve software productivity, is a research programme costing ECU 500 million (0.54 billion dollars) over five years.

ESSI will reply this autumn to the invitations to tender launched in the framework of the European ESPRIT II research programme and which should be adopted at the beginning of next year. The programme involves Europe's main specialist research centers, both public (INRIA [National Institute for Research on Information and Automation] in France) and private (the six main European computer manufacturers: Bull, ICL, Nixdorf, Olivetti, Philips and Siemens), about twenty of Europe's largest producers of integrated circuits, as well as the aerospace industries, who are among the principle users of these systems.

Although JESSI (ECU 3.5 billion) is a much more costly programme than ESSI, both will involve from the outset the principle users of spinoff from this kind of research during the last decade. The three large European groups—Philips, SGS-Thomson, and Siemens—thus form the inner circle of JESSI, which also involves more than a hundred American companies, who are keen to have access to European sources of components.

ESSI should also benefit from the ongoing research projects in the field of software engineering, the most extensive being the EUREKA projects EAST led by Cap Gemini Sogeti; and ESF, the software engineering house, notably including SEMA Group; not forgetting the last ESPRIT project, Atmosphere. These three projects together amount to about 450 man-years.

With JESSI and then ESSI, the Community should consolidate European recovery in computer technologies, which by the year 2000 should become the leading economic sector, with 7.5 to 8 percent of GNP, overtaking the agro-food industries, the current number one, leaving the automobile sector for behind.

DEFENSE INDUSTRIES

French, FRG R&D on Optical-Fiber Guided Missiles

89AN0241 Paris ELECTRONIQUE HEBDO in French 22 Jun 89 p 8

[Article by Pierre Arlot: "Tomorrow's Missiles May Have Optical Fibers"]

[Text] The use of optical fibers may permit "blind" missile launches (i.e., with the target out of sight): Euromissile (a French-FRG joint venture between Aerospatiale and MBB) has already proved the feasibility of the principle.

Wire-guided tactical missiles are already in use, but fiber-guided missiles may well appear in the near future and take over. Developing a tactical weapon capable of striking a target even though it is not located in the field of vision of the firing station (e.g., tanks or helicopters hidden behind a ridge) would be the major advantage of using an optical fiber—an umbilical cord unwinding behind the missile right from the start of the launch. A joint venture between MBB and Aerospatiale is already well under way with the Polyphemus project (named after the one-eyed cyclops the valiant Ulysses had trouble with during his many travels).

The first phase of the program, called Polyphemus-Demo and conducted by GIE Euromissile, an association between Aerospatiale and MBB, began in early 1984 and was to demonstrate the dual principle of missile guidance and the transmission of video images from an

on-board camera, all through an optical fiber. Antitank wire-guided missiles already exist, ranging from the SS10 to the current MILAN and HOT.

In the specific case of HOT/HOT2, the data are transmitted only in the direction of firing station to missile. During the flight, the missile is kept on the line of sight by an automatic servo-control system: The IR detector picks up infrared radiation emitted by the missile tracer and measures the angular deflection between the remote-controlled missile and the line of sight. This line is maintained manually on the target by the gunner. The deflection signals are transformed into metric deviations, which are then used to determine the guidance orders to be transmitted to the missile through the electric remote-control wire.

Possibilities for Indirect Firing

The optical fiber, on the other hand, can transmit much more information: television or thermal camera images, inertial references and other flight information in one direction, and piloting commands in the other. Other advantages including the possibility of indirect firing, because the operators can remain out of sight of the enemy; battlefield reconnaisance from the missile; identifying and then attacking a target; and resistance to electromagnetic jamming. The missile also costs less, because all the system's "intelligence" (image processing and expert systems) is located in the firing station and is generally protected from destruction. Moreover, the device can be modified as improvements are made.

As part of the project, an SS12-derived experimental missile fitted with a CCD camera (visible range) has carried out flights of about 7 km, including target tracking and hitting. Polyphemus firing operations require two pilots. In the first phase, just after firing, one pilot guides the missile in its ascent phase (about 10 seconds) by aligning the tracker with the sighting reticle which is driven by a preset movement; the second pilot is specifically in charge of the movements of the camera located in the missile head and mounted on a three-axis stabilized platform (range about 25 degrees). Once the tactical weapon enters its cruising path (altitude 150 m, speed 150 m/s) and a likely target has been detected, the pilot can engage the camera's automatic target tracking. After it has been determined that the target is to be destroyed, the pilot engages the missile's automatic target tracking (the first pilot is no longer involved).

Goal: 60-Kilometer Range

During the successful tests, the optical fiber used was a multimode fiber (dynamic passband: 100 MHz for 6.5 km; attenuation: 4 dB/km) linked to electro-optical converters in both the missile and the firing station. In order to eliminate crosstalk, optical links were made among different wavelengths in both ascending and descending directions (850 nm from firing station to missile, and 1,300 nm in the opposite direction).

For the future, Euromissile is planning on a range of about 60 km by transmission through high-yield optical fiber (monomode fiber with a throughput in excess of 100 MB/s) in the 1,300-1,550 nm window; an experiment has already shown that a camera can transmit an excellent image with very low attenuation through an optical-fiber coil of more than 60 km. In order to permit night firing, the current camera should also be replaced by an infrared camera.

Several applications have already been planned. In particular, a fiber-guided missile (Polyphemus SM) could be fired from a submarine, submerged to a depth of several hundred meters, at submarine attack helicopters or planes. The system could also be used for reconnaissance missions deep into enemy territory.

French Military Processors Described

89AN0242 Paris ELECTRONIQUE HEBDO in French 22 Jun 89 p 8

[Article signed P.A.: "French Military Computer Science Still Going After Equipment"]

[Excerpt] French military processors (FMP) are going to invade the new-generation missile-launching nuclear submarine SNLE-NG. No fewer than 30 FMP will equip what already appears to be one of the gems of the French Navy of the 1990s and the year 2000. Let us recall that, after consultations with the Navy in 1986, SAGEM, with Electronique Serge Dassault as subcontractor, was chosen to develop the FMP, which is now going into large-scale production. It was standardized through a contract from the French Government (the Electronics and Data Processing Directorate, CDE), intended to define a machine based on the 68020 microprocessor and organized around the general communications bus VME-M (military version of the VME bus), which is currently being standardized (GAM-T-104 standard). With a power of 1 million instructions per second, the FMP is a 32-bit multiprocessor computer, for which ESD has developed a macrohybrid central unit integrating onto a single component the processing unit (1.2 million operations per second) and the memory (1 MB)—the central parts of the FMP—and a central unit in the Double Europe standard format. The adaptable boards that make up the FMP are made using three different technologies: macrohybrid, dual-in-line (DIL) components on epoxy circuit, and leadless chip carrier (LCC) and hybrid components on ceramic circuit. The FMP can be connected to any local military digital data transmission network.

The SAGEM FMP computer has thus already been selected for equipping not only the new-generation nuclear submarine (for instance, in the SGN-3D navigation system and the SYTAC tactical system), but also the Orchidee ground monitoring stations. The central units developed by Electronique Serge Dassault were selected for equipping the AMX-Leclerc tank and the countermeasure systems of the F-16 (Carapace), Mirage 2000,

and Rafale. Furthermore, ESD is developing, again with SAGEM and under DEI contract, the CMF-AIR computer, a more powerful computer (6 million instructions per second) destined for the new-generation airplanes (in particular the Rafale).

Fiberoptic Area Networks Are Coming

As regards military local area networks, matters are also developing fast. The ESD digital-system division is working on the current Digibus and 1553B buses, which operate at 1 MB/s. The Digibus, which is based on the French interservices GAM-T-101 standard, is used in all the major programs of the various armed services, in particular the recent HADES launch system, the AMX-Leclerc tank, and the SNLE-NG submarine. The Digibus 2, an extension of Digibus which should have improved overall performance by the addition of a high-speed channel (16 MB/s), was selected for the SNLE-Q272. The same applies to the STANAG 3910 bus, an extension of the 1553B bus, which will be installed in the ACE Rafale and the European Fighter Aircraft (EFA).

In this field, optical fibers should make their appearance with the future Recital bus (deterministic [deterministe] Ethernet type), which operates at 10 MB/s and is destined for naval applications (nuclear aircraft carrier Charles de Gaulle). [passage omitted]

FACTORY AUTOMATION, ROBOTICS

FRG: Fraunhofer Institute Reports on Flexible Manufacturing Systems

89MI0309 Bonn TECHNOLOGIE NACHRICHTEN-MANAGEMENT INFORMATIONEN in German No 503, 19 May 89 pp 10-11

[Text] At the request of the Federal Ministry of Commerce, the Fraunhofer Institute of Systems Engineering and Innovative Research (ISI) has examined the state and prospects of automated production in the FRG. The main questions under study included:

- Does the use of new production technologies vary according to the individual sector and company size?
- ITo what extent are these differences due to different requirements in production technology solutions rather than to backwardness?
- Are the existing delays due to an inadequate supply of technology or to a lack of demand?

The main results are set out below:

- While almost two-thirds of manufacturing companies apply computer-aided systems and two-fifths use CNC [computer numerical control] machine tools, only about one-third of the companies currently work with CAD [Computer-Aided Design] and planning systems to program production [Zeitwirtschaft]. Only 10 percent use industrial robots and a maximum of 5 percent use flexible manufacturing systems.
- For all these technologies, applications vary according to the individual sector and company size, and the proportion of users ranges from 20 to 80 percent according to the type of technology. These marked fluctuations are partly due to the different stages of technology diffusion. In the initial stage there are almost no company size-related differences in the use of technology (this currently holds true for flexible manufacturing systems and industrial robots). In the intermediate stage, new technology is applied on a large-scale basis mainly by large companies, while small companies lag well behind (for example in CAD and computer-aided production programming [Zeitwirtschaft]). In the later stage of technology diffusion, the percentage of users among large and medium-sized companies increases only slightly, while small companies begin applying the new technologies on a larger scale (CNC machines and computer-aided production [Materialwirtschaft]).
- Regardless of this varying degree of application, the frequency with which technology is used increases in proportion to company size. When specific sectors are considered, companies specializing in mechanical engineering, automobile construction, electrical engineering, and plastics processing show an above average utilization of computer-aided production technologies
- The number of companies unable to exploit technology because of a lack of possible applications varies according to the type of technology. The failure to use CAD in the manufacturing sector is partly due to a lack of technological progress and to a limited possibility of major applications. In the case of computer-aided production [Materialwirtschaft] and production programming [Zeitwirtschaft] the ratio is 2:1. However, the failure to use CNC machines, flexible manufacturing systems, and industrial robots, where the ratio is 1:2, cannot be considered a sign of backwardness in the majority of cases.
- The possibilites of application are determined not only by the type of technology but also by company size and the industrial sector. As far as company size is concerned, the smaller the company the less likely it is to use computer-aided manufacturing technology, but no corresponding need to catch up is felt in this category. The untapped exploitation potential of a given technology increases in proportion to company size up to medium-sized companies, and then declines constantly, to reach a minimum in large companies.
- As regards technology in specific sectors, the steel engineering, wiredrawing, and woodworking industries make relatively limited use of computer-aided production technologies despite the existing potential. Many mechanical engineering companies feel the need to catch up, even though almost all the lines of technology in this sector are used to an above average degree. The electrical engineering and automobile sectors have a high number of users. Unlike the

mechanical engineering sector, most of these companies have already installed new manufacturing technologies. The textile, shipbuilding, and to some extent the iron, tin, and metal products industries are not behind in this respect, despite the relatively low number of users. However, they present fewer opportunities to apply these technologies.

- In four-fifths of the companies that do not use new technologies despite their potential usefulness, negative company attitudes are to be blamed. The main obstacles are lack of information and inadequate experience in the planning and introduction of computer-aided manufacturing techniques. Insufficient advantage is taken of the information available owing to time constraints, lack of interest, and incorrect procedures. For small companies in particular, the conversion required to introduce a new technology is another obstacle to the use of CAD and flexible production systems. Economic considerations are not as important as information and conversion problems.
- The inadequacy of international standards and the limited range of available technology have not been the main reason for the delayed introduction of technology. The larger companies that have already introduced different elements of computer-aided manufacturing technology are faced with a lack of standardized interfaces. This creates difficulties when they try to achieve integrated solutions.

MICROELECTRONICS

SGS-Thomson Lays Out Strategy for Growth

89AN0202 Paris TELEMATIQUE MAGAZINE in French Jun 89 pp 18-20

[Article by Jean-Francois Jacquier: "SGS-Thomson: The Flea in the Elephant's Ear"]

[Text] In order to survive, the French-Italian company SGS-Thomson—the second-largest European chip manufacturer (with a 26-percent growth rate in 1988)—must join the ranks of the world's 10 largest companies. One of its assets is the "transputer," a very-high-speed 32-bit microprocessor.

Grow or die: In the merciless world of electronic components manufacturers, dominated by the Japanese behemoths (50 percent) and by the major U.S. groups (40 percent), the tiny French-Italian firm SGS-Thomson Microelectronics (STM) does not have much choice.

For the company, whose management team is split between Gentilly, a Paris suburb, and Agrate, near Milan, this will be the year of double or nothing. In order not to jeopardize its chances for survival, it will have to maintain a growth rate of about 20 percent. This is a real challenge at a time when experts forecast another sharp decline in a market whose jagged cycles always turn out to be particularly murderous for this profession. During the last crisis in 1985-1986, the Americans lost their leadership to the Japanese in this way. Pasquale Pistorio, 52, director general of SGS-Thomson—the number two in Europe behind the Netherlands Philips, but only in 12th position worldwide—will not have an easy task.

But the last chance for eventual French and Italian—that is, European—independence in the highly strategic industry of electronic components rests on the shoulders of this dynamic Sicilian manager, a graduate of Turin Polytechnical College honed in Motorola's tough school in the United States. The stakes are enormous: Chips—the heart of computers and telephones, of television sets and robots—are to modern communications what steel was at the dawn of the industrial age. A nation lacking expertise in these silicon chips, which comprise hundreds of thousands of transistors, is condemned to play a secondary role.

Worldwide Sales of $45 Billion

"The semiconductor industry is still in its infancy, as was the automobile industry in 1923," explains Jean-Philippe Dauvin, economic research director at SGS-Thomson. With worldwide sales of $45 billion, the industry represents only 7 percent of the value of electronic equipment, but 100 percent of its performance. It is not by accident that Japan has invested heavily in this field, charging below-market prices to eliminate competition. In 25 years, Japan will have the oldest population in the world. It must therefore fight for maximum productivity. But the productivity is the result of machines comprising electronic parts, which, in turn, produce electronic goods. "The components industry is an infrastructure for autonomy," Jean-Philippe Dauvin summarizes, "and we are building the future at SGS so that our children will not be slaves to the Japanese."

"Easier said than done," Pistorio repeats. The problem is that, in spite of its 18,000 employees, 8 research centers, 18 design centers, 21 production sites, 59 sales offices, and 600 distributors or representatives, all spread out over five continents, SGS-Thomson, with some 3 percent of the world market, weighs in at only a little more than one quarter the number one-ranked Nippon Electric Company (NEC). There are only two ways to succeed in this field: Be one of the major general suppliers and offer a full range of products, or retrench into the small technological niches left vacant because of a lack of important markets. Of the 250 companies currently competing throughout the world, there will only be 10 major groups left within 10 years, each with about 5 percent of the market, in addition to some 100 firms with no more than 0.5 percent each. Between these two camps, the medium-sized companies, including SGS-Thomson, will have disappeared. This is why, right from the start, STM decided to aim for the major league; in any case, this is the only way to contribute to Europe's technological independence, which is something of a "mission" for STM.

The reconquest will take place in several phases. It began in July 1987 with the birth of the company resulting

from the 50/50 merger of Thomson Semiconducteurs, a subsidiary of the French Thomson group, and SGS (Societa Generale Semiconduttori), a subsidiary of the Italian public holding company IRI. At the time, each partner held about 1.5 percent of the world market, an insufficient size for survival: The critical threshold had just increased suddenly from 1 to 3 percent of the world market. Moreover, authorities on both sides of the Alps were tired of financing the semiconductor industry in vain. Thus, deficits served as catalysts for a merger. Both companies were losing money: $31 million on sales of $436 million for Thomson Semiconductors, and $18 million on sales of $306 million for SGS. The similar background of the men also helped facilitate a partnership. The two main architects of the merger, Pistorio for SGS and Jacques Noels for Thomson, studied together in the United States. In 1980, Pistorio had left Motorola to try to rescue SGS, agreeing to a 50-percent cut in salary. Noels joined Thomson after 17 years with Texas Instruments.

There was an additional advantage for the new entity created in this manner: Right from the start, it had a solid base in North America owing to Thomson's purchase of the Texas company Mostek in 1985. SGS, in turn, brought to the marriage its Singapore plant, which remains a real "must" to this day. The average hourly cost of an operator there is no more than $5, versus $15 in Italy and $13 in France or the United States.

But Singapore is the exception. It could not prevent the charismatic Pistorio, who was appointed head of the new SGS-Thomson company, from having to launch a frenetic efficiency drive: Five plants were to be closed, some 2,000 jobs eliminated, and management reduced by one third. The goal was to turn losses into profits and reach, as soon as possible, a sales figure of $1 billion, which is considered the minimum survival threshold.

Rescue Merger

Mission accomplished: At the end of its first full fiscal year, 18 months after the merger, SGS-Thomson got out of the red. The 1988 results that have just been published by the French-Italian company show pretax profits of $2.2 million on sales of $1.08 billion. True, these results are still modest, but they follow losses of Fr 131 million. Above all, they show a growth rate of over 26 percent, proving the merger successful.

Although he may have won a battle, Pistorio has not yet won the war. "The relationship has been set up, but we've only covered half the distance," admits the feisty Sicilian boss. After the reorganizations and the race to the critical threshold, the hour of the real reconquest has struck. The second goal in SGS-Thomson's strategy is to become one of the 10 largest component manufacturers in the world. This will require an increase in market share from 3 to 5 percent and in sales from $1 billion to more than $2 billion by 1993. This time, however, Pistorio knows that he cannot count on the exceptional market growth that he benefited from last year: According to Dataquest analysts, the growth rate is expected to drop from 30 to 9 percent in 1989. The challenge can certainly not be met by internal growth alone. SGS-Thomson will have to rely on a policy of mergers and acquisitions.

Company-generated funds will not suffice in the face of such ambitions. On the average, the industry spends as little as 20 percent of its sales on research. Another critical point is investment in equipment (18 percent of sales, on the average) needed for the manufacture of circuits. A plant that cost $20 million 15 years ago now costs $300 million, or 15 times as much. And its useful life has been reduced from 10 to 5 years. There is no doubt, then, that SGS-Thomson management needs further injections of capital by their shareholder, Thomson SA and IRI. They will also have to launch a new productivity drive. Average annual sales per employee have already increased from $44,000 to over $62,000. But this figure is $80,000 in the United States and $100,000 in Japan.

Is This French-Italian Dream a Nightmare?

The most arduous task will, however, be the penetration of new markets. In fact, the problem to be solved is twofold. The first problem concerns the company's product line, where gaps have to be filled, in particular in dynamic memories (DRAMs) and very-high-speed 32-bit microprocessors. SGS-Thomson relies too much on dedicated circuits and application-specific integrated circuits (ASICs), which represent 41 percent of the group's sales but only 27 percent of the world market. Similarly, the computer industry, the foremost semiconductor consumer at the world level (43 percent of outlets), represents only 20 percent of company sales. The second difficulty concerns geographic coverage. Overrepresented in Europe (60 percent of its activity), SGS-Thomson is almost totally absent from Japan, although that country absorbs 40 percent of world production. "This is one of our strategic problems, as it is for other Western manufacturers," admits Pistorio.

Is the French-Italian dream a nightmare, then? A first attempt at answering these questions has just been made with the purchase of INMOS (third largest manufacturer of 32-bit microprocessors in the world), a subsidiary of Britain's Thorn-EMI, in early April. Pushing SGS-Thomson from 13th to 12th in world ranking, this acquisition has also given French and Italians access to a small technological miracle: the "transputer," a 32-bit microprocessor capable of carrying out 2 million operations per second. This unique device, which was developed by INMOS engineers, is beginning to make inroads in the data processing. Atari is about ready to bring out a work station for teaching based on the INMOS transputer.

Another type of products merger is the European JESSI consortium, linking SGS-Thomson with Philips and West Germany's Siemens, Europe's number three since 28 October 1988. This cooperation could constitute

another way to reach critical size by virtue of its research capability for next-generation memories.

This leaves the Japanese market. Mergers? It is a question of opportunity. Not with the big Japanese names, but rather with one of their important local subcontractors—OKI has been mentioned—which would open the market in exchange for a technological contribution. The INMOS transputer could very well be a door opener in this respect.

But in this battle of "mercenaries," in Dauvin's words, SGS-Thomson's most important long-term asset is Europe. It is an enormous potential market of 325 million persons who are still underequipped in electronics ($25 spent per person), whereas Japan, with $145 per person, has virtually reached saturation.

France Produces GaAs-Based Monolithic IC

89AN0301 Paris FRENCH TECHNOLOGY SURVEY in English Jul-Aug 89 p 7

[Article: "Gallium Arsenide Technology Now Operational"]

[Text] Designed by Telecommunications Radioelectriques et Telephoniques (Telephonic and Radio Telecommunications) (TRT), a first complex monolithic integrated circuit in gallium arsenide has been built in an industrial process. Circuits using this same technology will form part of the new generations of radio transmission equipment.

The circuit built is a wideband linear modulator (0.9 GHz to 2.7 GHz). It comprises 70 transistors integrated on a 4 mm^2 chip. It utilises submicronic technology (grid length 0.7 micrometer).

The TRT company, which four years ago launched an ambitious technological programme aimed at monolithic integration for UHF functions, is now showing that the system has come to fruition.

The success of this gallium arsenide design stems from:

- high performance simulation tools; together with mask production tools, they allow the optimum circuit to be designed in one fell swoop;
- a high-quality fabrication process associated with a library of models, ensuring stable efficiency.

SAT Develops HD Image Transmission System

89AN0302 Paris FRENCH TECHNOLOGY SURVEY in English Jul-Aug 89 p 11

[Article: "Multi-Media Station for Transmitting and Managing High Resolution Images"]

[Text] The Societe Anonyme des Telecommunications [Telecommunications Company] (SAT) has recently built a system for the transmission of high-definition [HD] colour images at medium speeds, since they allow in particular 64 kbits/s applications on Transcom and ISDN. These systems open the way to a large number of applications: interrogation of image banks, point-to-point image transmission, image broadcasting over a local network, transmission of fixed images for video conferences, and so on. The Telsat Prisme uses an entirely new technique of mathematical processing, in accordance with the latest ISO standard. Redundancy is no longer necessary, and data imperceptible to the naked eye are eliminated. As a result, the image to be transmitted takes up much less space, but is identical, as far as the eye can see, with the initial image. The latter, which measures 760 dots by 576 lines (according to the new digital standard) or about 825 k for a complete transmission, measures only 50 k, which is less than one bit per pixel. This system has two advantages:

- a data file can be of a reasonable size: In this way many new applications become possible on a PC with about 1000 images on a hard 50 MB disc;
- with faster transmission (5 seconds in high definition mode at 64 kbits/s) it is naturally more economic.

The Telsat Prisme consists of two work stations:

- an encoder/decoder acquisition unit to which a camera or scanner or any other image acquisition system can be connected;
- a decoding unit allowing interrogation either directly or through a transmission system.

These work stations operate on microcomputers. Other applications are being developed for the OEM market, such as image consultation terminals, which will make it possible to create, for example, new applications of shopping or making reservations at a distance. These systems represent an appreciable improvement on current applications of this type, which have poorer resolution.

The Telsat Prisme is of interest to all in communications and advertising involved with graphics or documentation; all those involved in the graphics chain—printers, photo-engravers, production companies, and so on—can communicate in record times and under conditions of exceptional reliability.

Telsat Prisme is marketed by the Satelcom International Company, a member of the SAT group.

CNET Developing New Electroluminescent Display

89AN0195 Paris ELECTRONIQUE HEBDO in French 1 Jun 89 p 13

[Article by F.L.: "Electroluminescent Screens Shatter Performance Records"]

[Text] Thanks to technology developed by the National Center for Telecommunications Studies (CNET) laboratories, the cost and electricity consumption of electroluminescent [EL] screens could be considerably reduced.

The feasibility of this technology has been proved; the ball is now in the manufacturers' court.

CNET laboratories at Bagneux have just demonstrated the feasibility of a memory-equipped EL screen, developed according to the so-called photoconductor and electroluminescence (PCEL) process, which should make it possible to bring the cost of EL screens down to a level comparable to that of liquid-crystal-display (LCD) flat screens. While conventional EL screens require high control voltages, PCEL screens can be controlled by inexpensive complementary metal-oxide semiconductor [CMOS] integrated circuits of the same type of those used in LCD screens. The manufacturing process chosen uses equipment already on the market. Because the luminance obtained is greater than in conventional EL screens (up to 600 candelas (cd)/m^2), this technology also offers new alternatives for polychromy. CNET has so far developed a demonstration prototype with 64 x 64 pixels at 0.33-mm intervals and an effective area of 18 x 18 mm^2. On the face of it, nothing in this process should prevent the manufacture of larger screens. The laboratory is currently looking for industrial partners. Research is proceeding on a global level, since there are no French specialists in EL screens.

Bistable Concept

CNET has been working on EL screens for more than a decade. After having adopted direct-current screen technology, the laboratory turned to alternating current applied, inter alia, to thin-film dielectrics. Memory-equipped PCEL screen technology was developed later, as a result of collaboration with the Ecole Polytechnique's PMC laboratory. PCEL screens require a high (270 volts) permanent operating voltage between line and column electrodes, but they are controlled by small variations in voltage. The process consists in inserting photoconductive [PC] thin film of an amorphous hydrogenated silicon/carbon alloy in a thin-film EL structure.

The combination of the two films has both electrical and optical properties, because they are serially connected to the same power supply, and the PC film is exposed to the light emitted by the EL film. As long as the voltage applied to the PC film's terminals remains below a certain value, it receives no light from the EL film and therefore retains a large part of the voltages. As soon as the voltage exceeds the emission threshold of the EL film, it emits light. The resistance of the PC film and the voltage at its terminals drop. In return, the voltage at the EL film's terminals increases and approaches the applied voltage: The device lights up. A slight voltage reduction suffices to switch it off.

This process thus requires a permanent holding voltage on the whole screen, so as to place all the pixels in the bistability zone of the characteristic curve. However, the on/off state of each pixel is achieved by only a small variation in the control voltage at the electrodes: 15 volts for column electrodes and 45 volts for line electrodes (conventional EL screens require control voltages of 60 and 220 volts, respectively, on columns and lines).

The visual characteristics of this screen are the following: a luminance of 600 cd/m^2; a contrast greater than 200:1 (the PC layer provides a dark background, thus enhancing the contrast); a 150-degree viewing angle; and no flickering if pulse frequencies are greater than 1 kHz.

Moreover, the PC film allows information to be displayed directly on the screen using light beams in the place of controls. For example, the image of a projected slide or a message can be reproduced on the screen by means of a light pen if the screen is kept under its holding voltage. However, these operations can be performed only once: The image cannot be erased and replaced by another without the use of the screen controls.

By extrapolating the results obtained with the 64 x 64-pixel prototype, CNET has evaluated the performance of a 640 x 400-pixel PCEL screen with a 195 x 122 mm^2 display. The average luminance is projected to be 325 cd/m^2 for a standard consumption of 11 watts, a 3-milliampere line current, a 0.5-milliampere column current, a switched line voltage of 45 volts, and a switched column voltage of 15 volts.

1.6 Watts for 50-cd/m^2 Luminance

A version with a lower luminance of 50 cd/m^2 (still double that of conventional EL screens) would need a standard consumption of 1.6 watts (one-tenth that of conventional EL screens), a 0.5-milliampere line current, and a column current of less than 0.1 milliamperes. Intermediate-luminance versions can thus be envisaged.

The screens can be manufactured using the conventional processes for EL screens and for amorphous-silicon solar panels (deposition of PC layer). The increased luminosity of these screens reduces the color-dependent yield problem of luminophors. It is possible to envisage pixel structures with different subpixel sizes for each luminophor so as to obtain similar luminosities for different colors.

ADVANCED MATERIALS

GDR: Nanoceramics Fictile at 180 Degrees Centigrade Produced

23020080p East Berlin TECHNISCHE GEMEINSCHAFT in GermanNo 3 1989 pp 12-13

[Text]Using a new type of preliminary treatment, researchers at the University of Saarbruecken have succeeded in making ceramic materials fictile, even at 180 degrees Centigrade.

The size of the basic ceramic constituents is crucial to the deformation of a crystalline material. For a long time, the technology employed grain sizes of a few micrometers. For the first time, the researchers at Saarbruecken have achieved a grain size which is 1/1000 that size. Particles that size are easier to move about. The material becomes elastic at relatively low temperatures and can be shaped with little effort.

Up to now, the broad technical application of ceramic materials, for example, as heat- and pressure-resistant materials in automotive technology, has been limited by brittleness and the concomitant difficulty in processing.

The scientists at Saarbruecken achieved the smaller grain size by vacuum depositing the ceramic metal oxides in a vacuum and in a protective gas atmosphere. At very cold recovery stations—196 degrees Centigrade—the ceramic particles are cut to nanometer size.

Complicated ceramic components can be produced more easily using the new preliminary treatment. Quite possibly, nearly all hot parts in an internal combustion engine or in gas turbines could be repalced with ceramic material or could be fashioned entirely from ceramic material. The heat-resistant nanoceramic material allows higher combustion temperatures, thus improving engine efficiency. Moreover, the light ceramic, with its high insulation resistance, may permit drastic reduction in the proportion of heavy metallic alloys used in power plants.

AEROSPACE, CIVIL AVIATION

AUSTRIA: Update of "AUSTROMIR" Joint Space Venture

23020079p East Berlin NEUES DEUTSCHLAND in German1-2 Jul 89 p 10

[Text]At present, November 1991 appears to be the target date for putting the first Austrian in space. The joint USSR-Austrian space venture, dubbed "Austromir", will allow an Austrian cosmonaut to spend about a week working in the Soviet manned space station, MIR. The joint venture is to be undertaken on a commercial basis, Austria being thus obliged to pay the Soviet space agency, GLAVKOSMOS, around 85 million Austrian schillings. This sum will defray the costs of the space launch, cosmonaut training and the transport of Austrian scientific instrumentation into space.

Once aboard the MIR space station, the Austrian cosmonaut will be involved with 14 different scientific experiments. Nine of these have to do with medical or physiological considerations such as the effect of weightlessness upon attitudinal and postural reflexes, neural and muscular fatigue, mental functions during the adaptation to the space environment and the improvement of dosimetric control [not further identified] in space. Other exploits include physics, materials science and remote sensing experiments.

Apparently, there is a possibility that one of the new modules slated for completion in late 1989 could be used for the Austrian cosmonaut's work in space. The new modules, which can be accommodated by MIR's multiberth docking configuration, are to be tailored to experiments in biotechnology, crystal growth, medical research and the needs of extravehicular activities.

COMPUTERS

GDR's 8086 Microprocessor-Based 16-Bit Module Described

23020074 East Berlin NACHRICHTENTECHNIK-ELEKTRONIK in German No 6, 1989 pp 217-219

[Article by B. Hoier; F. Menge; Report from Humboldt University in Berlin, Electronics Section]

[Text]To support the transition to 16-bit technology, a single-card computer is being introduced, which can be coupled to an 8-bit system. Depending on its equipment, the computer has available 128 kbytes up to 1 Mbytes of RAM. The coupling to the 8-bit system is located on the card. With this module, an 8-bit system with a K1520 bus can be expanded to a full-scale 16-bit computer. The computer card is based on the 8086 microprocessor. Many applications can be implemented, for example, implementation of a CP/M 86 system.

1. Preliminary Remark

Within the framework of computer-supported signal processing, there is a series of tasks which can no longer be satisfactorily accomplished with 8-bit microcomputer systems. Among many other tasks these include e.g. filter operations, function transformations, statistical procedures, and the operation of fast peripherals. Personal computers with the MS/DOS and CP/M 86 operating systems are suited to simulate or to perform such operations on a laboratory scale. The upgrading of existing 8-bit computer technology with 16-bit supplementations is a sensible task in this connection. Furthermore, if the above tasks are to be solved in proximity to the process, suitable computer modules and a matching software system are required.

The objective is to develop a computer module with the 8086 microprocessor (can be supplemented with the 8087) and a matching software concept, that will be useful for many applications. The module is usable as:

- 16-bit supplement for 8-bit computers with K1520 bus [1],[2],[3]—implementation variant for CP/M 86 and MS/DOS with utilization of the 8-bit side as a peripherals control [4] and—coprocessor card (also several of them at one control computer)
- 16-bit central unit for the computer with the MS/DOS and CP/M 86 operating systems
- User system with specific software for signal processing.

The circuit concept is emphasized and it shows what mainly affects the design of a universally usable 16-bit computer with little hardware complication. The associated software concept contains the technical program aspects that are necessary for this. Application possibilities will be presented in the last section.

2. Circuit Concept

The circuit design of the computer module is oriented towards minimizing circuit complications. Supplementation with other modules is possible through two bus connectors.

The block structure of the module is shown in Figure 1 and it can be subdivided into the following functional groups:

z Generation of the clock pulse, processor logic and processor z Memory z Coupling to the 8-bit bus.

A clock pulse generator generates the unsymmetrical clock pulse that is needed for the 8086 processor. The choice of the quartz frequency is guided by the processor and memory switching circuits that are used. The card was tested up to a clock pulse frequency of 8 MHz. In order to be able to use an 8087 math coprocessor, the system is operated in its maximum mode. A bus controller is needed for this purpose, to generate the required control signals. Since the 8288 switching circuit is not available, the required component functions are simulated by TTL switching circuits (see Figure 2). The control signals can be generated from the processor status lines S0 through S2, the address lines A13 through A19, which are in intermediate storage, and the clock pulse. The following statuses are decoded from the status lines [5]:

- I/O read
- I/O write&Instruction fetch
- Memory read
- Memory write
- Inactive

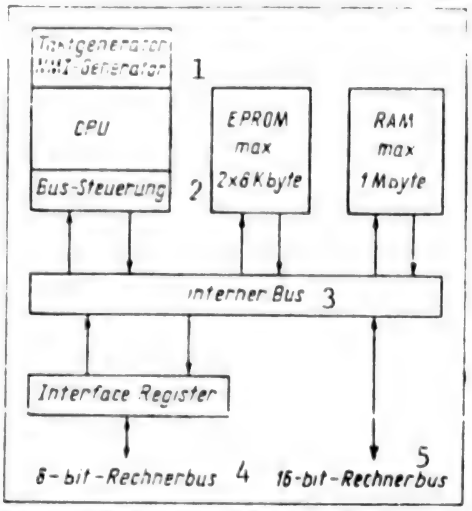

Figure 1: Block circuit diagram for module

Key: 1. clock pulses generator, NMI generator—2. bus control—3. internal bus—4. 8-bit computer bus—5. 16-bit computer bus

After the end of the inactive signal, a strobe pulse (ALE) for the address registers is generated in the following pause time of the clock pulse. [see Figure 2]

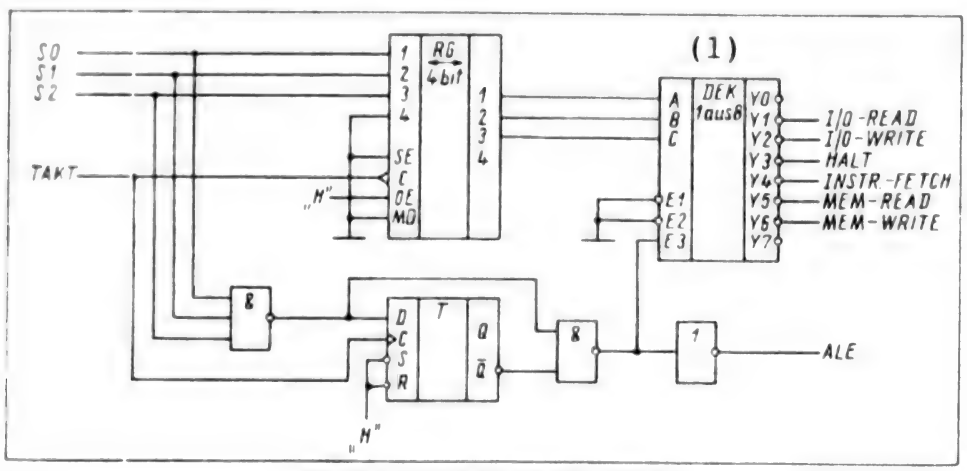

Figure 2: Circuit for the bus control

Key: 1. out of 8

$$V_R = ((n_R \cdot T_{SYS})/T_R) \cdot 100\%$$

T_{SYS} system clock pulse
T_R refresh clock pulse
n_R clock pulses for refresh

The bootstrap loader and other resident program components can be situated on two EPROM switching circuits (2764) in the uppermost address regions of the computer.

Sixteen or respectively thirty-two units of 64 Kbit or 256 Kbit switching circuits are needed for the dynamic RAM of the module. By selecting the RAS signals, the two RAM banks can be distinguished on the address line A19. By means of the CAS signal, one distinguishes between low-byte and high-byte. Address registers are necessary to separate the address and data bus lines that are operated in time multiplexing. The address registers with tristate outputs are simultaneously used for switching the RAM addresses.

The refresh function of the RAM switching circuits is guaranteed by the processor through the periodic triggering of an unmasked interrupt. 128 or 256 successive RAM cells are read with the interrupt service routine. The time load on the system can be calculated with the following equation:

With a system clock pulse frequency of 8 MHz and a refresh clock pulse period of 4 ms, the refresh function needs about 4 percent of the CPU time. This value justifies giving up a complicated circuit to generate a transparent RAM refresh. It is possible to block the refresh process so that certain program components can be executed without interruption.

Through the 16-bit bus that is available at the bus connector, the system can be supplemented by other modules, such as e.g. input and output units for fast data transfer, graphics display controls, or coupling modules with more 16-bit computer cards.

Data are exchanged between the 8-bit system and the 16-bit system via two 8-bit registers, whose status can be interrogated. The registers can be read and written by both systems. The 16-bit system here operates so fast that the status interrogation on the 8-bit side is needed only at the beginning of a transfer. If the block length is known, one can work with block transfer instructions (INIT, OTIR). As a result, the use of a dual port RAM would yield practically no gain in time.

The concept presented here is characterized by compromises in designing the RAM refresh and the data exchange. However, a powerful 16-bit computer system with many uses can be implemented with little hardware complication, by using the programming system explained below.

Software Concept

For meaningful use, program components are needed for the following main points:

- Activities after the reset procedure
- Implementation of the RAM refresh
- Operation of the 8-bit - 16-bit interface
- implementation of operating systems

```
o z80:    push    af              ;    output from the Z80 computer
stat80:   in      a, (status8)    ;    to the 8086 module
          and     1
          jr      nz,stat80
          pop     af
          out     (data8),a
          ret
i z80:    in      a, (status8)    ;    input from the 8086 module
          and     2               ;    to the Z80 computer
          jr      nz,i z80
          in      a,(data8)
          ret
```

Figure 3: Z80 Assembler Routines for Data Exchange

```
o 86:     push    af              ;   output from the 8086 module
stat86:   in      a, (status16)   ;   to the Z80 computer
          and     1
          jr      nz,stat86
          pop     af
          out     (data16),a
          ret
i z86:    in      a, (status16)   ;   input from the Z80 computer
          and     2               ;   to the 8086 module

          jr      nz,i z80
          in      a,(data8)
          ret
```

Figure 4: 8086 Assembler Routines for Data Exchange

After the reset signal, the following steps must be performed on the 16- bit side:

- Loading the starting address of the NMI routine (for refresh)
- Initializing the processor
- Starting the operating system and/or the user program.

The NMI routine consists of 128 or respectively 256 instructions "MOV AX,AX", and must be situated in the ROM. Neither flags nor register constants are changed when this routine is executed.

The software needed to operate the interface is very simple and is limited to status interrogation and to the writing or reading of the data ports. This is done according to the same schema on the 8-bit side and the 16-bit side (see Figures 3 and 4).

The greatest flexibility is achieved if only a bootstrap loader is situated on the EPROM switching circuits, which loads a program file from the 8-bit computer and then executes this program. For example, this may be a task-specific program which uses the single-card computer as a coprocessor in a multi-computer system.

A meaningful application is the implementation of 16-bit operating systems. The CP/M 86 operating system can be emulated if a CP/M 80 operating system is already running on the connected 8-bit system. Except for a few exceptions, there is an equivalent on the 8-bit side for every system call under CP/M 86. Consequently, these need to be forwarded only, via the interface, from the 16-bit side to the 8-bit side. A coupling program runs in the 8-bit computer to implement data exchange between the interface and the CP/M 80 operating system. If only operating system interfaces are used in the subsequently deployed 16-bit software, an adaptation to the computer peripherals is completely obviated, since this has already been done in the 8-bit computer.

It is also possible to start up MS/DOS on the system. Work in this connection has as yet not been completed.

Many application problems can be solved on the basis of the program concept that has been indicated here. The following section shall provide some insight on this point.

4. Application Possibilities

Among the application possibilities of the computer module, which have been mentioned as objectives, the variant as a 16-bit supplement for an 8-bit computer was tested out in practice. The 16-bit module was used in two operating modes:

- After the system was started and an appropriate emulation program was transferred to the 16-bit module, the latter takes over the control function. The peripherals are connected, via the interface, to the 8-bit system. Under the presupposition that a CP/M 80 operating system has been installed on the 8-bit computer, it is possible to use the CP/M 86. Thus, CP/M 86 programs, such as TURBO 3, TURBO 87, SID 86 and the like are able to run. These programs provide the preconditions for effective development, testing, and implementation of signal processing tasks. Additional peripherals, such as e.g. CCD cameras and step-motor controls, can be operated directly by the 8086 processor.
- The 16-bit module is used as coprocessor. Laborious arithmetic operations are performed by this module. The 8-bit system furnishes the operands and receives the results. Several coprocessors can be used in one 8-bit system, since one module occupies only three I/O addresses.

The computer module with a CP/M 86 operating system was put to a practical test in connection with picture filtering and the processing of characteristics for the classification of photo-micrographs of electrode coking

Filter Type (3 x 3)	Time(s)	Filter Type (5 x 5)	Time(s)
Average	35	Average	55
Ranking	35	Sigma	245
Sigma	47	Linear	72
Gradient inv.	360		
Loc. statistics	40		
Graham	34		
Brown	34		
Laplace	10		
Sobel	10		

Table 1: Program running time

[6]. With a picture size of 128 x 128 picture points, the computer clock pulse frequency of 6 MHz, and using the programming language TURBO PASCAL, the program running times given in Table 1 were achieved for each filter.

The single-card computer was also used to simulate the learning behavior of neural networks [7]. Because the algorithms are very computation- intensive, the 8087 math coprocessor was tested. A comparison of processing times of comparable simulations, which are translated by the compiler programs TURBO 3 and TURBO 87, yielded reductions to 10 percent to 40 percent for REAL operations. With pure INTEGER operations, the processing time with the 8087 increased because of the different mantissa lengths of the compilers.

5. Summary

The module and its associated program system which we have presented are a favorable variant of the transition to a new microcomputer generation. The computer module takes into account the trend of expanding existing 8-bit computers with reasonable effort, to facilitate entry into concepts that are based on the 8086/8087 processors. The circuit concept strove for a compromise between universal applicability and little hardware complication. In terms of programming, the computer module is based on a bootstrap loader principle, which supports the configuration of the software structure that is needed for the specific task. The emulation of a CP/M 86 operating system is especially important here. With support of the then available software environment, an approach to the 16-bit technology becomes possible with good results. Despite the small amount of hardware and software complication, the power of comparable 16-bit computers can be achieved.

further development of the concept in various directions is conceivable. Thought is being given to converting the computer module when controller and driver circuits are available, also to developing and adapting peripheral modules, with the objective of implementing MS/DOS including standardized graphics formats.

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GDR's First 16-Bit Programmable Control Unit Described

23020064 East Berlin MESSEN STEUERN REGELN in German No 3, 1989 pp 119-123

[Article by Frank-Guenter Meier, R & D group leader at the Karl Marx Numerics VEB, Karl-Marx-Stadt: "SPS 7000—a New Generation of Stored-Programmable Controls

[Text]

0. Introduction

Stored-programmable control [SPS] has become an important element in automation technology. The increasing demands on automation systems with regard to the range of functions, system limits, power draw and reliability impose great demands on the control technology employed.

The SPS 7000 stored program control developed at Karl Marx Numerics follows its predecessor types PS 2000, PC 600 and MRS 700.

In the SPS 7000 a modular stored programmable control system is to be made available, in particular for the processing machine sector, which replaces the former control facilities by expanded function characteristics and improved utilization properties and extends the application possibilities for this category of controls. In so doing, the range of functions presented represents only the first upgrade phase of a continuous SPS line, which is to be permanently expanded in order to meet national economic requirements, taking into account the contributions of the international state of technology.

1. Structure of the SPS 7000

The SPS 7000 was conceived for the intermediate and higher performance range (up to 2048 input/outputs) and in modules. In so doing the following fundamental conditions were assumed:

- standard bus structure, corresponding to SAK-N 316/01 and 02[4]
- standard construction, 19" component utilization according to TGL 37270, printed circuit boards in multilayer technology in double-Europa format
- standardized interfaces to peripheral equipment (such as serial channel RS 232-C) both electrically and based on construction.

The intermediate and large stored-programmable controls are characterized by the fact that they can undertake extensive functions for digital processing of information.

This circumstance imposes greater demands both on hardware and software in order that the reaction time of the control does not increase greatly through these complex functions. At present the linking of a microprocessor with a logic processor constitutes an practicable solution. In the SPS 7000 a 16-bit microprocessor (K 1810 WM 86) is coupled with a special logic processor. The logic processor is thus responsible for processing all of the binary instructions, while the microprocessor is used for all tasks extending beyond that.

All the process input/output groups (PEA) are connected via the system bus to the central unit. This results in their having a free choice of plug-in location. The address input takes place in the input/output components themselves (Fig. 1).

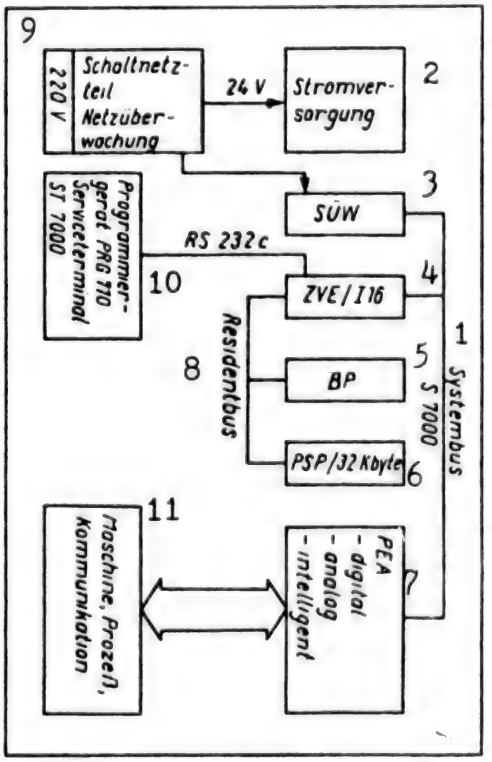

Fig. 1. Structure of the SPS 7000

Key:
1. System bus—
2. Power supply—
3. System monitoring—
4. Central processing unit—
5. Bit processor—
6. PSP/32 Kbyte [process control memory]—
7. Process intput/output—digital—analog—intelligent—
8. Resident bus—
9. Power supply; Power monitoring—
10. PRG 710 programming device; ST 7000 service terminal—
11. Machine, process, communication

The large upgrade phases for the control cannot be accommodated in one assembly unit. For the SPS 7000 another 4 assembly units are possible as expansion. Both linear and star-shaped bus extensions have been provided for.

The expansion of the range of functions and the resulting problems with respect to reaction time for the control have already been discussed. Attempts must therefore be made to keep time-intensive operations away from the central unit and to let them be carried out by decentralized (local) processors. The central processor then has only to take over the tasks of synchronization and data transportation. In the SPS 7000 this principle is consistently carried out through the creation of peripheral assemblies with their own intelligence for complex functions and by coupling all these assemblies via dual port

storage (DPRAM) to the system bus. By so doing all actions of the central processor toward the periphery can be made very efficient.

In the central unit itself the word processor and the bit processor are connected to the resident bus and work there together with the user program memory. Each of the processors is capable of controlling the bus. When the logic processor controls the bus, it is possible for the word processor to undertake genuine parallel work at its local bus and the system bus.

The user program is mixed in the program memory, meaning bit commands and byte/word commands are stored after one another and not separately. The operations code determines which of the two processors can process the waiting command. This test of the operational code can be undertaken by both processors, and switching only occurs when a genuine processor change must be undertaken.

By working in parallel it is possible, for example, to imbed an on-line diagnosis in the control cycle. Note the time differential between the processing of a logical command (1 µs) and realizing routines for the word processor from many commands (at least 800 ns/command), because the microprocessor is primarily designed to work in the application program.

2. Technical Parameters for Control

The principal parameters for the SPS 7000 are compiled in the table.

The variables mentioned are generally described as logical or binary variables, respectively. With the exception of the time function elements, the time commands and the counters, they are processed by the bit processor. The processing time for a logical operation amounts to 1 µs (with a memory requirement of one word (2 byte)).

In addition, byte or word processing is possible. The following parameters are relevant:

- Inputs, analog: max. 245 channels corresponding to 127 analog inputs
- outputs, analog: max. 245 channels corresponding to 127 analog outputs
- supported memories for byte/word operations with 2 Kbyte memory space
- number of implementable function components for processing byte/word- oriented variables: max. 128
- number of high-speed counting operations that can be accommodated (100 kHz): max. 16
- communication interfaces to the user or other stored-programmable controls through serial interfaces: max. 8
- possibility of splitting the user program into max. 20 parallel programs.

These operations are carried out or organized by the word processor. The main memory requirements for the addressable location of the user program includes 1 word (2 bytes) operations code and potentially necessary parameters. The main memory requirement is therefore very small for the user program, whose 32-Kbyte memory volume was still kept large. The instruction set (AL) is employed as programming language, and the basis for it is [3]. A circuit plan and function plan are being prepared.

Table. Technical Parameters for SPS 7000

	Number of channels	Number of variables
Address space bit processor divided into:		4096
Inputs, digital	max.254	2032
Outputs, digital	max.128	1024
Flags	max.254	2032
Flag expansion	max.254	2032
Traps	Max. 64	512
Error flags	max. 64	512
Time function elements (for circuit plan, Boolean equation)		
TH (10 ms ... 10 Min)		20
TS (1 s ... 16 h)		20
Time commands (TI, TR, TE, TA for operationally oriented programs)		20
Counters		40

3. Assembly Spectrum

The printed circuit boards have a double Europa format and have been manufactured using a multilayer technique. The front side has been supplied with a metallic cover ring, which has a galvanic connection to the assembly back plane. The electronics part is thus located in an electrically shielded space, which results in greater resistance to interference. The connection to the computer bus takes place via a 96- pin indirect connector and the coupling of processing signals through a 48-pin process-connector or through a miniature interface-connector. The following mounted boards (BLP) are used:

- System Monitoring—SUeW Monitoring of basic internal control signals, cycle time monitoring, temperature monitoring and ready status reporting, as well as error indication
- Central Processing Unit—ZVE I 16 16-bit microprocessor with peripheral circuits and memory (EPROM/RAM) for firmware, serial interface (RS 232-C) to connect programming/commissioning equipment
- BP Bit Processor Special processor for processing logical operations (AND, OR, EXCLUSIVE OR, allocation) and for special functions (jumps, also conditional; setting and resetting of variables; parenthesis (functions), interface to bus transfer during its ON-LINE state
- Program Memory—EPROM 32 KB

- Printed board assembly for storing user programs, 16 sockets for accepting EPROMs (2716) or CMOS-RAMs (U 6516). The use of RAM circuits only takes place during startup.
- Program Memory for Startup—SMOS 16 KB Memory assembly for use during the startup phase. One is enough for short control program lengths, otherwise 2 assemblies are needed.
- Digital Input Assembly—ED 1 16 external input signals, electrically isolated from one another, with a rated voltage of 24 V DC or 12 V DC, may be applied. The inputs can be used alternatively as either positive-logic or negative-logic (initiators).
- Digital Input Assembly—ED 2 This printed board serves to acquire and process digital processing information with a rated voltage of 24 V DC. It has 32 entries (4 channels) with a common reference voltage.
- Digital Output Assembly—AD 1 16 digital outputs with 24 V DC each, 400 mA with common reference voltage. The outputs are short-circuit-proof and in the event of a short circuit a message is sent to the central unit.
- Digital Output Assembly—AD 2 8 24 V/2.2 A outputs, short-circuit-proof, with common reference voltage. Feature: For a time up to 40 ms the outputs can deliver a 5.6 A current, which is important for activating inductive or capacitive users. During a short circuit a message is also issued to the central unit.
- Digital Output Assembly—AD 3 This is an assembly with 8 outputs. The power outputs are implemented with the GBR 12.3 relay. This results in the following parameters: Turn-on voltage 24 V to 220 V AC/DC, switching current 2.5 A, safety fuse. The contacts are designed with zero potential, meaning they have no common reference voltage.
- Digital Output Assembly—AD 4 This assembly has 16 outputs (2 channels), implemented with the RGT 13 relay. It is intended to switch low voltages and currents (1 mV to 30 V, 10 µA to 400 mA). It has no short-circuit protection.

The mounted boards mentioned here are voltage isolated, between the process part and the logic circuit, through an optical coupler and a 4- mm air and leakage path.

The following assemblies are available for analog signal processing:

- Analog Input Assembly—EA 1 This printed board has 16 analog inputs, which are digitized with a resolution of 10 bits. As a special feature it is possible to configure 3 inputs as differential inputs with adjustable gain (0.5 times to 250 times). The input voltage range is then +/-10 V, otherwise +/-5 V. Modification as +/-20 mA as current input is foreseen.
- Analog Output Assembly—AA 1 4 analog outputs with 12-bit resolution are available. The signal configurations are adjustable: +/-5 V, +/-10 V, +/-20 mA. At the present time the analog assemblies have no voltage separation.

The following intelligent assemblies have been included in the system so far:

- High-Speed Counter Input Assembly—EZ 1 Hardware counter with a limiting counting frequency of 100 kHz. 2 32- bit counting channels are available per assembly. The counter is selectable through 24-V input signals or it is possible to connect IGR D or E. Simple cut-off axes can thus be realized.
- Intelligent Communication Controller—IKC This is the assembly for communication between control and user or between controls. It has two serial interfaces (RS 232-C, IFSS). Because of the free programming capability, the most varied equipment (terminal, PC, printer, etc.) can be connected.

Additional assemblies are:

- Bus Extension Unit—Receiver/Driver In order to extend the bus from one assembly application to another, the BVEE and BVET boards are used. The distance can amount to up to 15 m.
- Power Supply Each assembly unit contains its own power supply corresponding with the mounted boards that are used (for example +/-15 V for analog assemblies). DC/DC transducers with a rated operational current of 24 V are employed. Based on the serial interfaces used (RS 232-C) and the equipment that can be coupled to them, the power supply must correspond with the status of an extra-low safety voltage. A 220 V/24 V/20 A (40 A) switching network is used.

4. Project Planning

4.1 Peripherals

The assemblies needed should be selected and the channel adresses determined according to the control task. From the sum of the assemblies the information will be obtained as to which expansion level (one to five expansion chassis variants) the control needs (Fig. 2). The following equipment is available:

One-expansion chassis variant with 11 connections for peripheral assemblies

Two-expansion chassis variant with 10 + 16 = 26 connections for peripheral assemblies

Three-expansion chassis variant:

- linear with 10 + 15 + 16 = 41 connections for peripheral assemblies
- star-shaped with 9 + 16 + 16 = 41 connections for peripheral assemblies

Four-expansion chassis variant

- star/linear-shaped with 56 connections for peripheral assemblies

Five-expansion chassis variant

- star-linear-shaped with 71 connections for peripheral assemblies

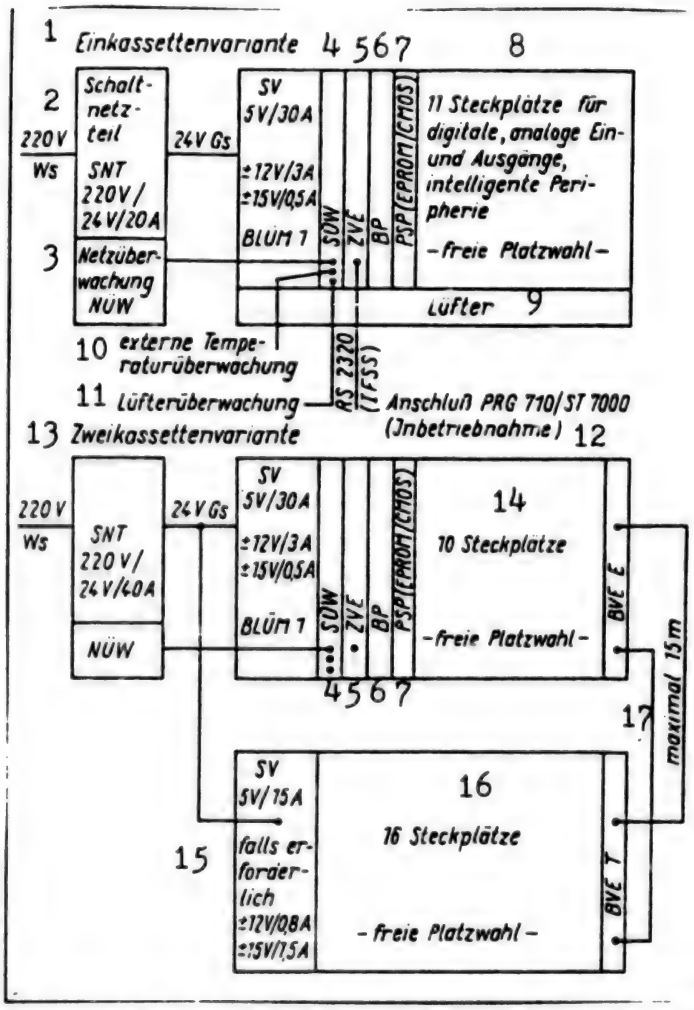

Fig. 2. One-Expansion-Chassis and Two-Expansion-Chassis Variants of the SPS 7000

Key: 1.One-Expansion chassis variant—2. Power supply—3. Power monitoring—4. System monitoring—5. Central processing unit—6. Bit processor—7. SPS (EPROM/CMOS)—8. 11 slots for digital, analog inputs and outputs, intelligent peripherals—free location selection—9. Fan—10. External temperature monitoring 11. Fan monitoring—12. PRG 710/ST connection (startup)—13. Two-expansion-chassis variant—14. 10 slots—free location selection—15. if neede—16. 16 slots—free location selection—17. Maximum 15 m

4.2. Core Image Storage

The core image storage (image of the process interface) is 1023 bytes (channels) in size. Thus, the bit processor can only access channels 0 to 511 (4096 bit). The user must allocate correspondingly large memory areas to the individual types of variables. With no gaps in the arrangement of input/output channels, block transfer between periphery and memory is possible.

4.3. Program Memory

The central control program memory has a maximum size of 32 Kbyte (16,384 commands), implemented by means of an EPROM plug-in circuit card (memory type U 2716). During startup the use of pin-compatible CMOS- RAMs is possible or can be undertaken through separate CMOS plug-in circuit cards.

5. Control Program Development and Process/Program Startup

A program package capable of running on the PRG 710 (Fig. 3) programming device is available for program development and startup. It has

- editors for acquisition of the block of values and the control program
- translator
- programm linkage
- startup program
- EPROM programmer

All data are stored on diskette. The number and the addresses of variables are combined with the WERTE-BLOCK dialog program and the projectable periphery of the stored-programmable control entered.

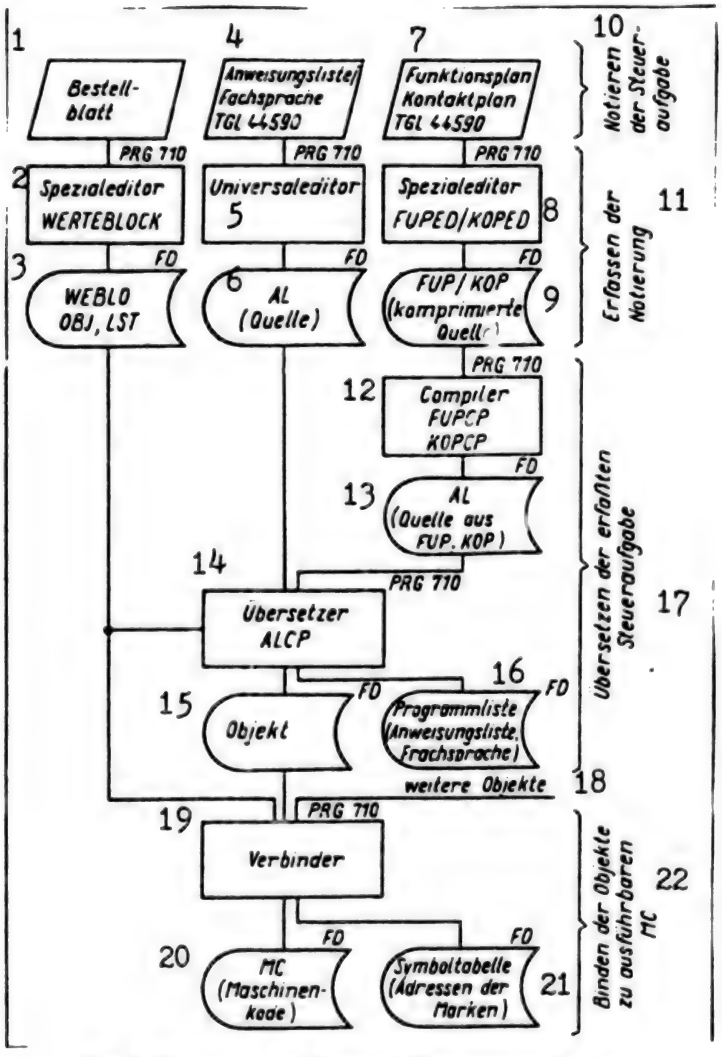

Fig. 3. Projection and Program Development for the

Key: 1. Instructor sheet—2. Special editor WERTEBLOCK—3. WERTEBLOCK OBJ, LST—4. Instruction set, special purpose language—5. Universal editor—6. Instruction set (source)—7. Function plan, circuit plan—8. Special editor—9. (compressed source)—10. Notation of the control task—11. Acquisition of the notation—12. Compiler 13. Instruction set (source from FUP, KOP)—14. Translator—15. Object—16. Program set (instruction set, special purpose language)—17. Translation of the acquired control task—18. Additional objects—19. Connector—20.MC machine code—21. Table of symbols (addresses of flags)—22. Combination of objects into executable machine code

The control task can be noted separately in modules as a list of statements vertically or horizontally (Boolean equation). When using a defined flag supply, retranslation of the machine code and thus corrections in the program memory of the SPS are possible. In using symbolic flags and variables, corrections in the source modules must be acquired. The ALCP translator translates the sources in the object code. The program linkage binds the value block and the object module into an executable control program. This program can be loaded with the INBET startup program from the programming device in the program memory (RAM) of the stored program control, or EPROMs can be programmed with the EPROM programmer.

For error search or "on-the-spot" startup it is not always necessary to work with the PRG 710, but it makes sense to use the significantly smaller and lighter ST 7000 service terminal with the SERVICE program package. Its **startup functions** are: Retranslation: Stored-programmable control editor (changing, inserting, deleting, relocating)—Translation to machine code—Setting mode.

The **operational modes** of the SPS are:

Basic State:

When a startup device is connected or during turn-on error diagnosis the SPS assumes the basic state. The basic state is designed for diagnosis, startup of communication from/to the process and for transmitting the control program.

Single-step Operation:

Starting up the control program when the process is turned off. A command or the control program is executed to an address. The starting address can be set by default.

Cyclic Operation:

Starting up the control program, in which the control program is interrupted after processing the cycles input at the start (computation of the cycle time possible). The process can be switched on. (SPS reads out operational readiness via the systems monitor.)

Test Operation:

Operation with functions for process startup (indicators, control, interrupt, logging data).

Process Operation:

Mode of operation, which, with unconnected startup device and error- free turn-on diagnosis, is automatically assumed after startup or reset. After acknowledgment of operational readiness by the process, the PPO control program is started.

Functions for Process Startup:

Starting up the process takes place in the operational mode TEST. The following have been designed as functions:

Display of Variables

The contents of the variables chosen are displayed once or constantly. The transmission of data and the display on the startup device run parallel to processing of the control program.

Control of Variables

The contents of the variables can be controlled once or constantly.

Logging

Either the 8 last states of the parallel programs or the states of 8 binary variables (or one channel, respectively) can be logged. Logging takes place at each change in status.

Interrupts

Interrupt conditions can be program status addresses (EA command) or states of a maximum of 8 binary variables each. If the fulfillment of an interrupt condition is indicated, the processing of the user program can be halted.

6. Fundamentals of the Programming

6.1. Binary Operations

Binary operations permit Boolean combinations and the assignment of binary values. In Boolean equations the operands are processed in s equation order (AND before OR, parenthesis).

The following operations are possible:

U	AND connection of one variable
UN	AND connection of a negated variable
O	OR connection
ON	OR connection of a negated variable
X	non-equivalence XN equivalence
U(	open AND parenthesis
O(	open OR parenthesis
)	closed parenthesis
)N	parenthesis closed, negation of an expression in parentheses
S	setting of a variable
R	resetting of a variable
=	result allocation to one variable
=N	allocation of the negated result

Up to 15 levels of parentheses are permitted.

6.2 Operations for Program Organization

Program jumps dependent on the value of a binary variable or the result of an operation, are implemented trough unconditional jumps, chip calls and input/output requests.

There is no special "program end" command with implementation of an input/output and jump to a program beginning. If cyclic processing of the program is necessary, an input/output request and an uncondit.onal jump to the beginning of the program must be written at the end of the program. The following **program branches** are possible:

SP Jump, unconditional SPV Jump for variable with value = 1 SPVN Jump for variable with value = 0 SPB Jump for result with value = 1 SPBN Jump for result with value = 0.

Zero operations are:

DEL deleted operation NOP no operation.

Input/Output Prompt:

EA Input/Output of processing signals

Each control program must contain at least one EA command. For several active parallel programs the EA

command means transition to the next control program. The input/output of processing signals is not prompted until all active control programs but one EA command have been processed. After input/output of the processing signals, the processing of the control programs is continued at the retrieved address of the first control program.

6.3 Function Modules

Function modules are parameterizable routines of the operating system, which are carried out by the microprocessor. They can be modified or supplemented by the user. For example, function modules are used to service the intelligent EZ 1 and IKC assemblies.

Calling a function module:

BAF Name Parameter 1, ..., Parameter n

Program Modules

Program modules are subprograms to be defined in the control program, but which are not parameterizable, in the programming language of the SPS. The maximum nesting depth of program modules is 8.

Calling a program module:

BA Name

To return to the calling program: BE (module end).

6.4. Parallel Programs

A maximum of 256 parallel programs may be noted in the source program. A parallel program is translated as an autonomous module. All flag names are valid only in the module. A maximum of 24 parallel programs can be managed at the same time in the SPS. The PPO parallel program is instantly active after initializing the control. All other parallel programs must be activated with the command AP. A parallel program can only deactivate itself or all others (jointly). It should be noted that at least one parallel program must be active in the SPS.

Conclusion

A memory-programmable control with modular construction for the upper performance range is presented. With it, increasingly more complex functions in addition to Boolean processing are implemented. The programming language is to enable the user to program his tasks without special knowledge of microprocessors, and, through the corresponding support on the part of the startup technology, to operate the SPS simply and rationally.

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Overview of Leipzig Spring Fair 1989

23020069 East Berlin RECHENTECHNIK-DATENVERARBEITUNG in German
No 4, 1989 pp 5-12

[Article: "Increasing Efficiency of PC Technology—Complex Applications Solutions With Greater User-Friendliness"]

[Excerpts] In the GDR's 40th year the Leipzig Spring Fair [LFM] brought together about 9,000 exhibitors from all over the world. The theme was flexible automation with special emphasis on integration of mechanical engineering in the area of machine tools and processing machines on the one hand and electrical engineering/electronics on the other. For that reason, a great deal of space was devoted to CAD/CAM technology—including the requisite software—in conjunction with 16-bit and 32-bit technology.

The 1989 LFM exhibited a comprehensive offering of hardware and software from at home and abroad. Outstanding in this regard was the effort to present user-oriented and adaptable applications in exhibit halls 15, 17, and 18. Although this was the area designated to focus on computer technology, there really was hardly any exhibit hall where the personal computer was not present.

The leading producer of GDR computer technology, the VEB Robotron Combine, announced at the LFM that in 1988 it produced 534,800 typewriters, 57,400 personal computers, 175,000 disk drives, and 113,000 printers. Not only was the GDR's national economy thereby supplied with considerable information technology equipment, but there were also substantial exports to 60 countries. Some significant fair exhibits that we consider representative and worth presenting are discussed below.

Applications Solutions and Software From Robotron

In exhibit hall 15, the VEB Robotron Combine participated in the joint center for electrical engineering/electronics and mechanical engineering in its offer of thoroughly interlinked solutions in computer assisted systems as well as systems and equipment for complex rationalization and automation of operational processes.

The presentation was divided into the following three levels: 1. Production control and management with management, planning, balancing, and accounting.—2. Preparation of production with development, design, and technical preparation.—3. Implementation of production with direction of production, quality testing, and shipping/transport.

User- or sector-oriented solutions in computer, typing, and printing technology including software and measurement technology could be seen upstairs in exhibit hall 15. Computers in various configurations demonstrated user programs from many areas of the national economy. Some of the different applications solutions should be presented in somewhat greater detail:

GRAMOS-16

GRAMOS-16 is a open modeling system for elaboration of CAD/CAM solutions on 16-bit computers and assists the user with an efficient user layer in operational processes.

The centerpiece of the GRAMOS-16 modeling system is the generation of product data models for technical preparation for production. For design preparation, the basic functions for modeling, archiving, and representation of geometric and technical objects (assemblies, component parts, geometric elements) are presented.

The data structures created within the framework of these DP design processes are not however limited to geometric data but also include production technology data.

These geometric structures enhanced using production technology data are used by the production engineer as data models with the help of which he transforms the design data into the technical foundations for production within the framework of technical preparation for production. To perform these tasks, GRAMOS-16 is offered in two major sections:

- a CAD section (GRAMOS-GEOMETRY)
- a CAP section (GRAMOS-ALPHA).

Hardware Requirements

PC EC 1834, AC 7150:

- 512 or 640-K main memory
- Hard disk and disk drives
- Graphics screen, graphics tablet, plotter, graphics printer, DCP operating system

GRAMOS-16 is offered by Robotron Berlin.

On-Line Coupling of EC 1834 and EC 1057

In exhibit hall 15, various possibilities for coupling terminals to a lead computer were demonstrated. Several workstations based on 16-bit PC's or workstation computers of types EC 1834 and AC 7150 were linked via on-line coupling with an EC 1057 EDP system in the test center at VEB Robotron Plant Construction downtown.

The GIFEMA software solution was demonstrated on a CAD workstation with the EC 1834—consisting of a basic computer with two floppy disk drives and a 50-MB hard disk, keyboard, alphanumeric screen, color graphics monitor, matrix printer K 6314, and graphics tablet K 6405 (connected via KIF adapter with the large computer on Gerberstrasse). With it, the Berlin School of Architecture, a cooperative partner with Robotron in Leipzig, presented static calculation methods which are used in architecture and mechanical engineering. In a second exhibit, software specialists from VEB Robotron Plant Construction demonstrated their DCS/DCP data communications system, which they had already shown successfully at the Dresden Software Fair last November. It permits the use of workstations or PC's as end-point nodes or intermediate nodes in computer networks. This system was demonstrated by coupling two EC 1834's via ASK adapters and linking them in turn to the EDP system in the test center via KIF adapters. The VEB Robotron Project Dresden presented a third solution, consisting of the coupling of an A 7150 workstation computer directly to the EC 1057 on Gerberstrasse via a V.24 interface.

CAD/CAM NILES

CAD/CAM NILES is a comprehensive computer assisted solution for bent parts made from sheet steel. Implementing this software package, the entire computer assisted process for bent parts made from sheet steel was demonstrated by a flexible automation production system.

CAD/CAM NILES is composed of the following complexes:

- Geometry capture and geometry representation as a 3-D model
- Joining of parts in 3-D
- Working with technical shape elements in 2-D (development of sheet steel parts)
- Generation of corrected developmental views, visual control of the part under assembly conditions as a 3-D model
- Derivation of sketch views from the 3-D model
- Integration into the company-internal organization sequence with standard controls
- Transfer of the parts into a geometry memory with a retrieval system
- Geometry controls and geometry conversion for NC programming
- Transfer of the geometry from the CAD system into the programming system for technical preparation for production
- NC programming of component parts based on the geometry from the CAD system and automated sequences for machine tool selection, optimization of process technology and collision observation
- Daily selection of parts from the production databank and optimum arrangement of component parts on a metal sheet.

EC-NET for EC 1834's

Local area networks [LAN's] are groups of computers connected by adapters and cables in a limited area up to approximately 1,000 meters. These transmission paths do not fall under the control of the postal service. The advantages of LAN's are high transmission rates and low error rates. The EC-NET networking system is designed for configuring LAN's based on the EC 1834. To operate EC-NET the computers must be equipped with the following hardware components:

- K 8625 LAN controller
- TCR K 8601 transceiver (media connection unit)
- Transceiver cable to link the LAN controller and transceiver
- Coaxial cable (75-ohm).

The EC-NET LAN is topologically configured as a line bus; the access procedure is CSMA/CD.

The EC-NET program package was demonstrated using the DCP 3.30 operating system. The interface between the EC-NET and the LAN is the NETBIOS interface which is widely distributed internationally. With it, other program packages that use this interface can also be run. The following operations can be implemented with an EC-NET:

- Transmission of messages, use of network diskettes and network directories
- Receiving and storing of messages
- Access to shared disk capacity and printers on the LAN.

Depending on the configuration, components such as virtual disk systems, data protection, access controls, and operator communication among others are immediately available when the network is initialized and can also be used with "normal" DCP commands (e.g., DIR, COPY, etc.).

Software for Users and Developers

AIDOS/M-2 DCP

AIDOS/M-2 DCP is an AIDOS product into which all experience from previous implementations and applications has been combined. AIDOS/M-2 DCP is particularly suited to scientific data processing. For this, AIDOS/M-2 DCP offers extensive and efficient means for effective storage, upkeep, and purposeful retrieval of variable length records such as listings of books, journal articles, research reports, market surveys, product lists, patent documents, travel reports, medical results, and many other accumulated documents. AIDOS/M-2 DCP significantly simplifies retrieval of such records with the assistance of thesauri and classifications.

AIDOS/M-2 DCP is also designed as a satellite system of AIDOS/VS (for mainframes). AIDOS/M-2 DCP runs on 16-bit PC's under the DCP operating system or compatible operating systems.

TEXT 40K

TEXT 40K permits operator communication in German and in Russian as well as processing of German and mixed-language texts. Roman/German and Cyrillic character sets are available.

Texts can be output by TEXT 40K on any matrix printer. In addition to standard word processing operations and simple operator control, TEXT 40K offers the following applicational advantages:

- Automatic hyphenation in German and in Russian
- Conversion and processing of "TP"/TEXT-30 files
- Processing of TEXT-40-SCP files in the DCP operating system and vice versa
- Generation of tables of contents and indexes
- An installation program which can be called up at any time
- Boiler-plate and form-letter processing
- Merging of tasks (selection of specific addresses) for multiple use of groups of addresses in form letters
- Windowed display of file content directly from the file directory (for example, before execution of the print program).

TEXT 40K is implemented in C. It is designed for 16-bit PC's with at least 512 K of main memory with standard peripherals.

MORES DCP—MODULA-2-Based Development System

MORES DCP assists in the input of problems into the computer. As a rule, technical specialists who are capable of analyzing and describing the problem at hand are not experienced programmers. MORES DCP accommodates these people by supporting the graphics style for the design, implementation, and testing phases. MORES DCP also helps systems software developers by supporting structured programming. MORES DCP helps the developer apply software engineering discipline in design, implementation, and testing, which pays off with low "bug counts" and easy program maintenance. MORES DCP aids in software development using the MODULA-2 language. It was also developed using MODULA-2 and is therefore readily portable.

Basic Software for Artificial Intelligence (AI)

The 30 years of international R&D in the AI area have led to initial components which can now be applied in actual practice. Because AI increasingly distanced itself from the modes of operation of conventional EDP, it developed its own tools, methods, and techniques. Based on the LISP and PROLOG languages created in this process, the Information Science Center of Dresden

Technical University, within the framework of a cooperative program between Robotron and the university, developed the ETA-P DCP and ETA-L DCP systems. They provide a developmental environment and tool system for planning knowledge-based applications systems based on PROLOG and LISP.

K 6416 Compact Plotter

The K 6416 compact plotter is a drum plotter for ISO A3/A4 and ANSI A/B graphics formats, with a plotting speed of 300 mm/sec. With expanded margin mode, it is possible to create technical drawings with standard-sized margins and title block. Both white and transparent plotter papers as well as plotter films including projection films can be used for multicolor sketches. Plotting tools used are ink pens with fiber or plastic tips and stenciling pens. The pen carrousel can simultaneously hold eight plotting tools of different colors or line thicknesses for program-controlled exchange. The paper drum, the pen carriage, and the pen magazine are driven by step motors. Using the 14-K data buffer, a large part of the graphics to be plotted can be immediately transmitted in full from the computer to the plotter, freeing the computer for the next task during plotting.

New From the Communications Electronics Combine

The RFT communications system for office and factory automation displayed at the fair was part of a user solution in exhibit hall 15.

The centerpiece of this communications system which provides voice, data, text, and image communication in automated operation in conjunction with PC's, data-link devices, and modems with access to the telex and packet networks is the digital extension board NZ 400 D/384 with data capability.

It is not merely a communications system, but can also be used as a data PBX system by connection to the public data network via X.25 interfaces.

A LAN (using ROLANET) is set up by the VEB Robotron Combine using the digital connection of the NZ 400 D/384 extension board.

A newly developed microcomputer-controlled remote monitoring system for automatic monitoring of operating processes in printed wire board fabrication was introduced: A maximum of 96 matrixed video outputs can be distributed to 96 video inputs.

In addition to its modular configuration, potentials for integration of existing systems and the complexity of devices from other manufacturers are among the advantages to users of this system. The F 2000, a microprocessor-controlled teleprinter with the TE 2000 text processing unit and K 7222 screen unit, was introduced for the first time. The RFT transmit-receive printer thus becomes a modern office communications device which can be used as an office workstation for word processing.

Carl Zeiss Jena With New Circuits

The combine was present with exhibits which included the following: ZBA 21—efficient and highly accurate electron beam lithography systems for structuring masks and wafers in the production of VLSI circuits up to the integration level of the 4-mbit-DRAM AUR 2 (automatic mask repeater).

It is used for production of VLSI circuits (256-Kbit and 1-mbit level).

A universal software program for generation of operations programs assists in the adaptation using the higher level of automation.

The following highly integrated circuits and circuitry systems of Carl Zeiss Jena also attracted special interest: U 61000 DC12/U 61000 DC10. This 1-mbit write-read memory is the first circuit type developed by the combine based on NMOS technology in the 1-micron level. Because of its structure level (high packing density), the chip can be installed even in small standard cases.

The circuit will be used primarily in calculation and communications technology as well as in industrial electronics.

Another of the new or upgraded exhibits is the two-coordinate measuring instrument ZKM 01-250 CM. This device was coupled with other systems (including the laser testing system 200 and small testing machine KMM 60) for the objectives of CIM technology with new user software for 2-D and 3-D measurement problems of coordinate test methods (developed by GDR companies for the combine).

The ARCHIMEDES software system newly developed for it is used to process geometric data and is tailored specifically for the specifications/requirements of manufacturing technology. ARCHIMEDES can be transferred to other computers based on their market specifications. [passage omitted]

VIDEOTON's 20th Appearance at the Leipzig Fair

VIDEOTON has been represented by its products in the GDR since 1979. Since then, numerous computers have been installed in various application sectors. VIDEOTON takes care not only of the maintenance of its computers and peripherals—the user can also have the necessary software delivered along with them. Exhibited for the first time was a solution for integration of the Robotron EC 1834 computer with XT/AT- compatible VT 110 and VT 160 computers in a NOVELL LAN. Beginning in the second quarter of 1989, it will be possible to perform file transfers from the LAN to the Ethernet network of the VT 32 and R 11 via a gateway. Both the software and the hardware are included in delivery of this LAN solution for the 16-bit PC VT 110 (IBM PC/XT compatible) and VT 160 (AT compatible). The LAN software offering includes network software compatible with NOVELL Advanced NetWare 286 or network software compatible with the NOVELL System

Fault Tolerant NetWare 286. The following operations are included among the functions of the software:

- File handling with its own structure, which has higher speed
- Controlled access to shared files
- Generation of security backups of directories and file description tables.

Compatible VT 110 PC

The IBM-PC-compatible VT 110 and VT 160 PC's are new VIDEOTON computers. With them, many programs created for the MS-DOS 3.2 operating system can be run successfully. The VT 110 provides high storage capacity and fast data access. Data can be stored in a maximum of 4 data memories, which can be diskette, Winchester, or streaming tape memories. Display takes place on the monochrome graphics or color graphics monitor. The basic unit of the PC includes the chassis, the main board, the 150-W power connector, the 5.25-inch disk drive, and the printer cable. The chassis can accommodate 6 long and 2 short boards, 2 half-height floppy disk drives or streamer units as well as 2 Winchester disk memories, likewise half-height. The main board has the following elements: 8000-2 microprocessor with 4.7/8 MHz clock signal, 649-K RAM, ROM BIOS (Basic Input Output System).

PC/AT-Compatible VT 160 PC

The VT 160 computer is fully compatible with the IBM PC/AT. Data can be stored in a maximum of 4 data memories, which can be diskette, Winchester, or streaming tape memories. Display takes place on the monochrome graphics or color graphics monitor. The main board has the following elements: 80286 microprocessor with switchable clock signal (6 and 8 MHz), 640-K RAM (expansion to 1 MB possible), 32-K ROM BIOS, 16 IT inputs, 7 DMA channels, and keyboard interface. Expansion of the working memory to 1 MB can be accomplished by exchanging the 64-K units for 256-K units. A 3.5-MB memory board is used for further memory expansion. An 80287 numeric processor may be built in as an option. VIDEOTON presented its new product line of robotics technology in Leipzig for the first time.

Isotimpex

Bulgarian exhibits included:

- The CM 5307 magnetic tape storage with automatic tape feed (density of flux changes 63 bits/mm), data transmission rate 189 Kbytes/ sec., tape speed 3.176 meters/sec.),
- The ISOT 7200C video terminal,
- The SVIT digital image processing system (64-K RAM) with magnetic tape storage, floppy disk system, color screens and camera (for scanner and microscope), and
- The CM 511 mini-solid-state 300-MB memory.[passage omitted]

EAB With ICA 700 Industrial Computer Family for Flexible Automation

In exhibit hall 15, the VEB Electroproject and Industrial Plant Construction Berlin [EAB] showed a combination of automation devices: ICA 710.20 and ICA 710.30 industrial computers coupled with MRS 704, MRS 705, and S 2000 stored program controls supplemented by the EC 1834 PC and BDT 8902 operational data terminal as an example of a flexible automation system. Characteristic of the production management technology is the DP linking of devices, systems, and technologies (production technology, communications technology, data processing) into one unit, i.e., the strategy and implementation for the control and monitoring of the entire manufacturing process. The hardware base consists of

- Devices for operational data capture, stored program controls, CNC and industrial robot controls on the end near the machines
- Stored program controls and industrial computers on the control level
- Industrial computers and universal computer technology on the management level.

The applicational range of the production management system extends from automation of large plants (e.g., automobile manufacturing) to small and medium-sized operations, such as the metal processing, household appliance, furniture, and food products industries, among others).

Production management technology forms the basis for computer integrated manufacturing (CIM).

ELWRO With Model M-2424

In addition to the standard configuration of the ELWRO 801 AT, which we presented at the time of the 1988 LFM, as we did its range of applications at the time of Infosystems 1988, ELWRO introduced its newly developed M-2424 modem. It is used for data transfer in LANs and has a transmission rate of up to 2400 bits/sec. and can operate in both synchronous and asynchronous mode pursuant to the following standards: Bell 103, 214 A, and CCITT V.22. It also operates using Microm's Network Protocol (MNP)—Class 3 for error-free data transfer. For this, the additional open architecture interface connector is used. This plug-type connector makes possible the future upgrading of the modem with additional transfer functions. For efficient and economical use of the data transfer lines, it includes a voice/data switch with which the existing connection can be switched from data transfer to voice mode. The M-2424 modem can be operated manually or with automatic answering, automatic dialing, and automatic monitoring of the connection to the telephone grid with pulse or frequency selection. The M-2424's operability can be tested in various modes: LAA (local analog loopback), LDL (local digital loopback), RDL (remote digital loopback), and audible connection test to verify the electrical connection. [passage omitted]

COMPUTERS

GDR: CAD/CAM Applications Software Described

23020070 East Berlin RECHENTECHNIK-DATENVERARBEITUNG in German No 4, 1989 pp 24-27

[Article by Karl-Heinz Bondick, Guenter Richter, VEB Data Processing Center, Magdeburg: "An Integrated Software Package for CAD/CAM Applications"]

[Text]In planning complex application systems dealing with distributed processing, the problem often arises of establishing technologically solid and effective connections between the various hardware and software components by means of supplementary development which sometimes can be expensive and complicated. Another problem that needs to be solved is to guarantee that central data which have been acquired once can be used all through the entire system.

The VEB DVZ Magdeburg has produced an integrated software package, which uses components of data management, data communication, and applications- oriented technical preparation for the efficient implementation of complex CAD/CAM projects, by means of the computer technology delivered by the VEB Combine Robotron. For about 10 years, the VDB DVZ Magdeburg has developed basic software and generalized applications software that is being used in all areas of the national economy of the GDR. From the very beginning, the development of software products was closely related to practically feasible possibilities of distributed information processing. Software systems that are known all over the republic and that have proven themselves in practical use are e.g. —the data base operating system DAFEMA for ESER (Uniform Electronic Data Processing System)-EDVA (Electronic Data Processing Equipment) /1/ - the file transfer system DATRA for data exchange between ESER-EDVA and 8- or 16-bit PCs /2/ —the software system RTV for computer-supported technical processing /3/.

The need for software and EDP performance has expanded in recent years. On the one hand, the mass use of ever more powerful personal computers is increasingly creating pressure for more powerful forms of distributed data processing, and on the other hand new requirements emerge more strongly from the CAD/CAM area, which are generally associated with the requirement of computer-supported control of complex processes. Software development at the VDB DVZ Magdeburg followed this trend by: - significant expansion of the power offered by established software components, - purposeful supplementation of existing software products by new ones, which make it possible to include modern technologies of information processing, and - a highly developed interface design, which secures the matching and effective interaction of individual software components and which offers convenient user interfaces.

What resulted was an integrated software package which facilitates the creation of all-round solutions with a reduced need for expertise and with maximum application support. Furthermore, the effective applicability of individual software products naturally remains, which guarantees a step-by-step expansion of application solutions.

Components of the Software Package - State of Development

Data Base Operating System DAFEMA with CAD/CAM Support

At this time, more than 60 businesses and far more than 100 installed data base systems use DAFEMA. It is therefore one of the most frequently used and centrally recommended ESER data base operating systems in the GDR. Applications use the extensive power of DAFEMA both in batch operation and in interactive operation under central TCAM control. Typical applications are:

- Information system for call numbers for regional telephone exchanges of the German Post Office - Managing and preparing for print all the telephone books in the GDR - Production control systems in machine construction and in the electronics industry - Inventory management systems in the construction of heavy machinery and motor vehicles - Management information systems - Data management systems for technical information.

Extensive applications experience is derived from this broad practical effectiveness. The cited businesses also transmit this experience for DAFEMA application to

- the German Post Office - Institute for Telecommunications in Berlin - VEB IFA Combine PKW, Karl-Marxstadt - VEB Electronic Components "Carl von Ossietzky", Teltov - VEB Measuring Equipment Works "Erich Weinert", Magdeburg - VEB Flow Machines, Pirna.

But at the same time, this experience is an important source for practically relevant further developments of DAFEMA, which are primarily directed towards CAD/CAM applications and the increased integration of PCs as smart data base terminals. The following important new capabilities, in addition to extensive system improvements, are available with DAFEMA 6.0 (Figure 1):

1. Storage and manipulation of composite structures

In addition to the previously physically separate storage of individual types of records in various relations, different types of records, corresponding to their logical linkage, can now be stored physically connected within one composite structure. Thus, effective storage of hierarchically structured data of technical or technological objects is feasible in DAFEMA data bases. This facilitates low-access process- related manipulations of complete objects in CAD/CAM applications. The individual types of records of an object e.g. headers and footers to

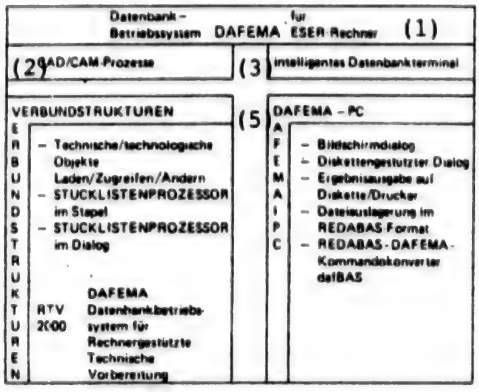

Figure 1.

Key: 1. Data base operating system DAFEMA for ESER computers—2. CAD/CAM processes—3. Smart data base terminal—4. INTERCONNECTION STRUCTURES: technical/ technological objects -load, access, alter; - PARTS LIST PROCESSOR in batch mode; - PARTS LIST PROCESSOR in interactive mode; RTV-2000 [computer-assisted technical preparation (system)]—5. DAFEMA-PC: VDU (visual display unit); - diskette support dialogue; - output of results on diskette/ printer; - transferring files to external storage in REDABAS format; - REDABAS-DAFEMA command converter dafBAS

describe a product or a technological process, can furthermore be evaluated as independent relations by means of the procedural DAFEMA language.

2. Functions for processing parts lists

Special forms of parts list processing that are traditional for data base applications have already been implemented on the basis of relational data storage by means of the procedural language. For data storage in composite structures, effective processors for parts list resolution in the interactive mode (e.g. product-related parts list and material applications list) as well as in batch processing (total parts list for a complete product program) are now being furnished, and the scope of their performance is being expanded in close collaboration with the users.

3. PC integration as smart data base terminal

Work-place related computer technology has been furnished at a greatly speeded up rate. This makes it necessary to use decentralized computer power in close connection with central data base resources. DAFEMA solves this problem with the component DAFEMA-PC, which includes the available 8-bit PCs (BC A5120/30, PC 1715) and 16-bit PCs (EC 1834, A7150) as smart terminals for working on data bases. DAFEMA-PC implements the following functions:

- Interactive mode on the screen with the DAFEMA data base while using diskette support for staticizing off-line prepared DAFEMA instructions on the screen as well as for storing the resulting data displayed on the screen, to be used for subsequent evaluation. - Diskette-supported interactive mode with the DAFEMA data base, where DAFEMA instruction sequences that have been previously stacked on diskettes are transferred to the ESER computer for execution, possibly in parallel with screen interactive mode, and where the results are retransmitted to the PC for storage on diskettes for subsequent evaluation. - Roll out of DAFEMA data stacks on the PC in the REDABAS format for decentralized evaluation and manipulation in the REDABAS environment. - Integrity protection of the DAFEMA data base, while changing the decentralized data stock by means of REDABAS, with the command converter DAFBAS, which translates the corresponding REDABAS instructions into DAFEMA instruction sequences. In a subsequent session, these instruction sequences, using diskette-supported interactive mode, accomplish the changes in the central data base.

These capabilities are offered by terminal connection via synchronous (BSC 3) and asynchronous (AP 62/64) transmission procedures. Thus, they also support simple formation of a distributed data base operation between the ESER computer and the PC.

4. Interfaces to the system of distributed processing DDS

Users of the system DDS /4/ can access a central DAFEMA data base by means of the global DDS request language. By incorporating arbitrary file transfer software in the technological execution process, a remote connection can also be implemented.

With the innovations that have been listed, DAFEMA, as a central data management system, is a dominating component of the integrated software package. To an even greater degree than previously, it supports the implementation of user solutions for processes that prepare and implement production, with centralized and work place-related technology.

Remote Data Processing and Computer Network Software

Software developments are connected with the implementation of the expanded system of remote data processing (DAFEMAB) under TCAM control, which in the meantime effectively support analogous processes in other enterprises and facilities.

ZNSP (Central Message Control Program) for the Central Control of TCAM Applications

The central message control program has the task of implementing remote access to various DFV (remote data processing) applications in complex DFV systems, on the basis of the expanded access method TCAM, and of controlling the message flow (Figure 2). It makes possible a variable and dynamic allocation of terminals to DFV user programs. As an essential application aspect, the time-shared collective utilization of lines and terminals by various users can thus be implemented. The

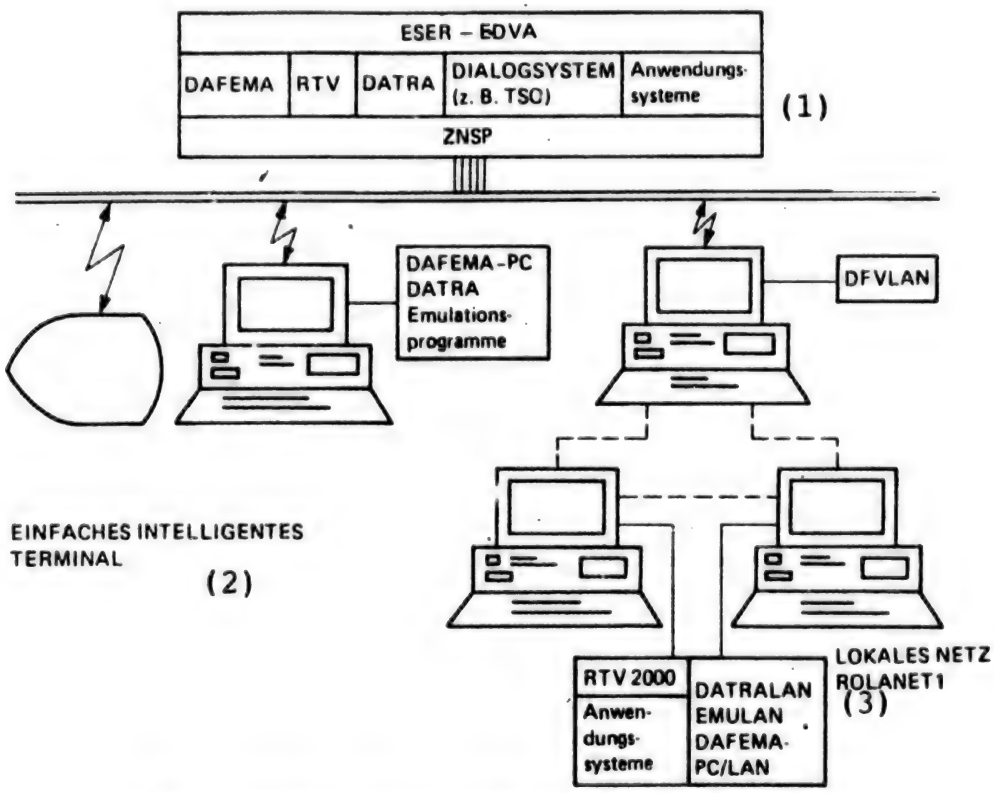

Figure 2. Integrated software package from the VDB DVZ Magdeburg
Key: 1. Application systems—2. Simple smart terminal—3. Local network ROLANET 1

allocation is initiated in the interactive mode by instructions from the terminal operator. ZNSP is advantageous primarily for such ESER computers on which several different DFV tasks are being processed as TCAM user programs, where the collaboration of many terminals with different tasks as well as a change of tasks are to be secured. In its current version, ZNSP supports collaboration with the application systems DAFEMA, DATRA, TSO, DAKS, ITS.

File Transfer Software DATRA

The file transfer system DATRA is already being used widely for file transfers between ESER computers and 8-bit PCs. It was supplemented by the capability of connecting the 16-bit technology (DCP operating system). The special performance characteristics of this technology were taken into account in the present software solution. All terminal connections can be operated both in the synchronous transfer procedure (BSC 3) and in the asynchronous one (AP 62/64).

Within the framework of distributed processing, DATRA does justice to the special technological situation and security requirements of larger computer centers. It can be characterized briefly as follows:

- Central control of the transfer system on the ESER computer using the ZNSP - File exchange (text or transparent data) in multi-user operation on the basis of prepared transfer jobs - Dialogue-oriented initiation, monitoring and control of the transfer by the terminal user - Transfer of the original data (sequential, mixed record length) with modification capabilities via exit routines of the ESER component and with data compression during the transfer - Error handling measures (file transfer protocol, user-controlled restart), display of the current transfer status, logging capabilities.

ESERLAN for Remote Connection of Local Computer Networks to ESER- EDVA (Electronic Data Processing System)

The use of the local computer networks (LAN) is directed, among other things, towards work place-related CAD/CAM applications. As a rule, there are requirements for the computational performances in an LAN, which require connection to the powerful ESER technology and particularly to the memory capacity of available ESER data bases. An integration of ESER computers as servers in LAN is possible only for such users as have available their own large-scale computer technology. However, many users use centrally installed ESER technology, by way of DFV, e.g. in the data processing centers of the VEB Combine Data Processing. For such groups of users, the remote connection of ESER computers and LAN by means of DFV can also be implemented and is technologically advantageous.

With ROLANET 1 /5/, the LAN device technology including the LAN basic software has been made available step-by-step to the PCs of the VEB Combine Robotron since 1988.

Consequently, respectively heterogeneous LANs with 8 and 16-bit PCs as work-stations could be installed. According to the present delivery status of ROLANET 1, the software product ESERLAN is at first available for remotely connecting a LAN (SCPNET), consisting of 8-bit PCs, to the ESER computer. Here, a LAN station as a so-called DFV station, is connected via the V.24 interface to the central TCAM control (ZNSP). The DFVLAN component works together with the ESER system via the synchronous procedure BSC 3. Through the LAN transport utility, it establishes the connection to several work-stations in the LAN. DFV- typical utilities are available for these LAN work-stations. These are known going back to the ESER-DFV, and have been adapted to the LAN protocol (Figure 2):

- DATRALAN for file transfer - EMULAN for ESER interactive work (emulation EC 7927).

In this way, it is made possible for the user of a LAN work-station to exchange files with the ESER computer at the technologically required times, to request information from the large-scale computer system, or to initiate there the processing of associated component projects. The expansion of ESERLAN anticipates, among other things, data base access to DAFEMA, leaning on the technology of the DAFEMA-PC component, as well as the incorporation of a 16-bit PC as DFV station or communication server.

CAD/CAM User Software RTV-2000

The well-established rationalization solution RTV for computer-supported technical processing has for more than 10 years been furnishing a powerful system of methods and programs for rationalization in the production-preparatory areas of the enterprises, by means of which successful applications were achieved in various industrial branches, such as e.g.

- Machine Tool Combine "7 October", - TAKRAF Combine - Gear and Couplings Combine - Petroleum/ Natural Gas Combine - Toy Combine

The associated results and experience flowed into the continuous further development of this solution, which was oriented towards the ESER computers. With the wide use of work-station computers and with the availability of modern communications technologies, for their interaction and their connection to mainframe computers, there opened up new possibilities of effective support by engineers and designers. For this reason, the product line RTV-2000 provides an innovative solution, which displaces decisive and time-critical tasks to the PC technology, and at the same time incorporates the most recent scientific-technical knowledge concerning production preparation.

Computer-supported technical preparation is operationally organized between production, planning, control, checking, and invoicing of production. The basic concern of RTV-2000 is to rationalize all the processes in preparation for production which have documentary support, to automate them, and to make available the various documentation/files for production planning and invoicing. PC work-stations for the designer, the engineer, the materials planner contribute towards the fast and economical generation, storage, and modification of technical documentation with, for example:

- work plan master cards - parts lists - work instructions - NC control information - drawings

as well as making these available for operational planning and management processes, which are largely supported by ESER projects. Due to the contextual interlinkage between the various subject-specific PC work-stations (8-bit PC for input/output functions and 16-bit technology), they can be advantageously combined as work-stations in an heterogeneous local computer network ROLANET 1 (Figure 2). Their collaboration with the ESER computer, which generally is connected remotely, is provided for mass storage as well as for a technological linkage to supplementary projects of ESER mass data processing. Within the integrated software package, there also is a close connection between RTV-2000 and a CAD/CAM data base based on DAFEMA.

RTV-2000 is a two-component software system divided into the generally valid basic solution and the operation-specific user solution which is based thereon. Adaptation to user conditions is implemented with program generators and user-friendly descriptive technical languages. It is also supported by copious methodological guidelines. An instant entry system provides the basic stage of the basic solution. By means of technical languages, variable possibilities of writing and defining the documentation are made available. The documentation can subsequently be processed with available editors. This work can flow into the printing of the documentation, among other things. For example, user programs, in the form of test processes, can be incorporated into the processing of the documentation.

The rationalization stage significantly increases the level of automation of technical preparation. Special languages for the engineering and technical description of the work pieces as well as of the engineering model of production form the basis for an all-round automated generation of documentation. By incorporating the description of drawing elements, the automation of document generation is also extended to drawings, through the connected drawing generation systems such as PCAD/CAMAD. Thus, the rationalization stage offers an advantageous starting point for a long term CIM strategy.

Interface Design Within the Software Package

Interfaces to link the individual components as well as user-friendly and transparent final user interfaces have a

high priority within the software package. These contribute towards user acceptance of an application solution that is based thereon. Interfaces are available for integrating various hardware and software components such as e.g. the ESER technology and PC terminals, and LAN, DAFEMA and REDABAS, RTV- 2000 and DAFEMA. While preserving expandability with manifold technological orientations, these can be incorporated into the specific user solution (Figure 2). The possibilities extend from the interactive mode of operation with simple terminals up to transfer orientation at work-stations of the local computer network as a basis of distributed processing. Naturally, they can also be used in combination.

The important efficiency aspect of the interface design is established by optimal throughput conditions (under the given preconditions), the inclusion of data transformations and compressions in the individual software components, as well as by extensive checking methods for functional reliability including error handling capabilities. To this are added measures which are more strongly oriented towards the conceptual world of the user. By means of simple screens (menus, templates, windows), and supporting high operating reliability in case of malfunctions, these secure a good user interface.

The richly variable and efficient modes of operation for the final user are sketched in Figure 2:

1. The following components are available for central ESER systems:

- ZNSP for central TCAM control - DAFEMA with system-intrinsic interactive-mode support (among other things as background mass memory or CAD/CAM data base for RTV-2000) - RTV/ESER with an interactive-mode interface via TSO/PTS (for selected mass data processing in the context of technical preparation) - DATRA as an ESER component for transfer implementation.

2. Interactive access to the central components via simple terminals such as AP 62/64 or EC 7925/27 or PCs with appropriate emulation software

- the procedural DAFEMA language, including DAFEMA language including the available template and menu support, where extensions of the instruction spectrum are permitted by way of user programs written in Assembler, PL/1, and C. - the technological support offered by DAFEMA-PC - the RTV command procedures

3. Transfer-oriented access includes smart terminals which, in the sense of distributed processing, also are important as autonomous work-stations:

- DATRA terminals with their associated command language as local end terminals of an opened file transfer system - DAFEMA-PC with instructions for transferring files to external memory.

4. Remote connection of local computer networks offers largely autonomous operating possibilities for decentralized application systems, with all the advantages of the LAN technology. The user-process-oriented CAD/CAM software RTV-2000 is available in the software package. It has system-inherent, manifold user interfaces for the work-stations concerned with technical preparation. Furthermore, DFV-typical services as linkages to the central ESER technology are available for RTV-2000 and also for arbitrary other application systems in the LAN. This is accomplished with the ESERLAN component, analogous to the connection of individual terminals.

The object data interface has special importance (because of its supervening character) within the software package for CAD/CAM applications. On the one hand, it is of great interest to the final user at an RTV-2000 work-station, since the processing of closed objects dominates in the area of technical preparation. On the other hand, it requires special handling between the central DAFEMA data memory and the decentralized RTV-2000 application, which implements in the object data storage in the REDABAS format. The following technology is supported in all-round object orientation:

- transferring data out from composite structure, from the central DAFEMA data base into a sequential file with object-related memory (DAFEMA roll-out instruction formulated interactively) - transfer to the decentralized work-station (transfer with DATRA or by using DAFEMA-PC) - decentralized, object-related roll-in of data (RTV-2000) - object-related processing (RTV-2000, REDABAS, or user programs) - return transfer to the ESER computer - object-related roll-in to secure integrity of the DAFEMA data base with a special DAFEMA instruction for composite structures. This secures the time-optimal exchange of changed objects at the memory location.

An integrated software package offers comprehensive support in the planning of overall operating solutions in the CAD/CAM area. This is aimed towards the distributed processing between central ESER technology and work place technology. Mutually matched, powerful, and also separately usable components secure step-by-step build-up and expandability of user systems. The VDB DVZ Magdeburg is continuously advancing this line of development. Contact the VEB Data Processing Center, Magdeburg, Sales and Procurement Department, telephone 594347, PSF 312, Magdeburg, 3010, if there is further interest and in connection with utilization.

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GDR's 16-Bit Microprocessors Described

Microprocessor U80600

23020071 East Berlin MIKROPROZESSORTECHNIK in German No.5, 1989 pp 130-131

[Article by Dr Dietrich Mandler and Dr Hendrik Berndt, VEB Microelectronics "Karl Marx" Erfurt, Research Center: "The Fast 16-Bit Microprocessor System U80600"; first two paragraphs are MIKROPROZESSORTECHNIK introduction]

[Text] Based on the VLSI technologies producible by VEB Microelectronics "Karl Marx" Erfurt, a new high-performance 16-bit microprocessor is being developed.

Design centers of user combines and other user partners, including Robotron Combine Dresden, Carl Zeiss JENA Combine, the Central Institute for Cybernetics and Information Processes Berlin, Electrical Instrument Works Combine "Friedrich Ebert" Berlin, Automated Plant Construction Combine Berlin, and Semiconductor Works Frankfurt (Oder), are participating and have made significant contributions to the development of the circuitry. The developmental goals for the fast 16-bit microprocessor system to be introduced were implementation of modern architectural features and achievement of downward compatibility with the USSR's 16-bit microprocessor system K1810.

Foreword

With the efficiency of its processor, the U80600 system represents a new generation of microprocessors produced by VEB Microelectronics "Karl Marx" Erfurt. It is characterized by the following features:

- Internal, virtual memory management
- Internal, efficient memory protection concept
- High-speed processing using two preprocessing mechanisms (on the byte and instruction levels)
- Efficient address computation using additional arithmetic hardware
- Increased data throughput (bus interface with 8 MB/sec.)

In addition, the U80600 system has significantly increased efficiency in its peripheral components. Expansion of the complex range of functions of the storage system and increased reliability and user-friendliness are achieved through highly integrated system components. These performance features distinguish the primary applications of the U80600 system in personal and industrial computers, in process automation, in workstation systems, and in communications systems, i.e., for operational conditions in which high processing speed and simultaneous processing of multiple tasks are required.

Scope of the System

The U80600 microprocessor system is designed from 20 components of which the basic ones are presented in Table 1.

Table System U80600

Type	Application
U80601	Microprocessor
U82720	Graphic display controller
U82530	Serial communications controller
U80606	Bus controller
U80608	Error checking and correction circuit
U80610	Programmable DRAM controller
DS82284	Pulse generator
U82536	Counter-/Timing- and parallel I/O circuit
U8272	Floppy disk controller
U82062	Hard disk controller

The system performance of the U80600 system is described below in detail through its components:

- U80601 Microprocessor
- U80606 Bus controller
- U80608 Error checking and correction circuit
- U80610 DRAM controller

The system may be expanded to include

- Bus arbiter
- DMA controller
- Arithmetic processor
- LAN components, and
- other multifunction peripheral circuits.

For a great variety of configurations, 8-bit address bus and data bus drivers from Semiconductor Frankfurt (Oder) and other circuits from the 16-bit microprocessor system K1810 WMxx are available to the user for expansion of the entire system.

With them, it is possible to set up a system configuration like that represented in Figure 1, which (equipped with floppy units, hard disks, LAN connections, etc.) corresponds to the established requirements of GDR's instrument industry.

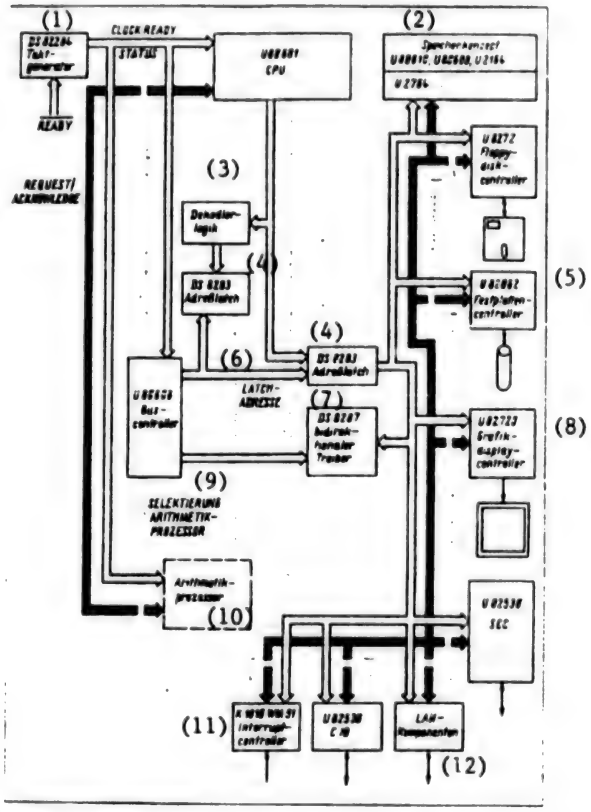

Figure 1. U80600 system configuration

Key: 1. Pulse generator—2. Storage design—3. Decoder logic—4. Address latch—5. Hard disk controller— 6. Latch address— 7. Bidirectional driver— 8. Graphic display controller— 9. Arithmetic processor selection— 10. Arithmetic processor— 11. Interrupt controller— 12. LAN components—

Microprocessor Features

Architecture

The high processor performance of the U80601 is achieved through four parallel processing units. The bus unit organizes access to memory and peripherals and data transfers with coprocessors. In addition, it handles DMA control (direct memory access). Byte-level preprocessing is likewise performed in this unit.

Combination of the preprocessing bytes into instructions occurs in the instruction control unit. For this an internal preprocessing mechanism is used which:—handles prefixes,—extends immediate operands,—and determines microprogram addresses.

The instruction queue includes three instructions. The execution unit is used for actual processing of instructions. It therefore contains the general purpose register, the arithmetic logic unit, other logic units for processing complex instructions, and the microprogram memory.

Address computation in the address unit occurs parallel to instruction processing. For this, an effective address within a segment is created for each bus cycle. A logical address is derived from it following application of protection mechanisms. This in turn is used to compute a physical address using segmentation. A series of cache registers containing data for segmentation and protection functions is present in the address unit.

Architectural Features

Virtual Addressing

The address space of the U80601 is partitioned into segments whose base address may be shifted into the physical address space if desired. Segments are allocated to code, data, and stack areas. Segment description takes place in turn through tables, so-called segment descriptor tables. The virtual memory space is defined by these descriptors as 1 Gbyte per task.

Access Protection

Task isolation occurs through allocation of an internal, local table of segment descriptors to each task. Among other things, these descriptors specify access rights, violation of which leads to trap functions.

As additional measures of protection for operating system functions, four privilege levels have been defined in the U80601. Program operation in the privilege levels and transfer to other privilege levels are supported by processor hardware.

Integrated Task Switching

The importance of rapid task switching mechanisms is quite significant particularly in realtime operating systems but also with multitasking and multiuser capabilities of operating systems. Therefore, in the U80601 a hardware-based task switching mechanism is implemented. The description of tasks again occurs via tables (44 bytes per task). A task switch with register save and register switch takes less than 21 microseconds.

Modes of Operation

The U80601 has two basic modes of operation: the real address mode and the protected mode. After initialization or system reset, the processor is automatically in the real address mode. Here, the U80601 has full object-code compatibility with the K1810 WM86. Real addressing occurs; the physical storage area contains 1 MB. A few new instructions have been added to the instruction set. The U80610 CPU runs significantly faster because of its improved cycle timing.

After the necessary descriptor tables are established, it is possible to change to the protected mode using a special switch instruction. There, the architectural features described, virtual addressing and access protection, are active. The working memory contains 16 MB, and architecturally dependent instructions have been added to the instruction set. The U80601 is optimized for this

mode of operation. The U80601 may support a coprocessor parallel to its address and data performance.

Brief Description of Selected Circuits

U801606 Bus Controller

The use of the U80606 bus controller increases the efficiency of the U80601. It decodes status signals and provides the bus system with the most important instruction and control signals.

Within the U80600 system, the U80606 is used for address latch control signal generation of the data transfer controller and for standard instruction output. Timing is controlled for two modes of operation (MMS-16-bus, local bus). Using two bus controllers, operation of the U80601 with two bus systems is possible through partitioning of the physical address space.

U80608 Error Checking and Correction Circuit

The U80608 error checking and correction circuit is a circuit designed to increase the reliability of memory systems. It is used for rapid detection and correction of errors in static and dynamic memory systems.

The U80608 is capable of processing 8 or 16 data bits and up to 8 check bits. By cascading a maximum of five circuits of this type, data words up to 80 bits wide may be processed.

U80610 DRAM Controller

The U80610 is a programmable DRAM controller for dynamic memory designs. It supports connection of 16-, 64-, and 256-Kbit DRAM's and is capable of managing an address space of up to 2 MB. The controller circuit permits RAM accesses without wait cycles and permits RAM initialization and programming of four refresh modes. Its use significantly reduces the hardware outlay required for managing dynamic memory.

With its two ports, the U80610 permits addition of dual port RAM structures with synchronous or asynchronous communication with the processor. The U80610 also has an ECC [error checking and correction] interface. With this, along with the U80608 error checking and correction circuit, it is easy to design large storage systems that generate error correcting code and eliminate correctable RAM errors during the refresh phase.

Compared to previous microprocessor systems (U880, U8000, K1810 WMxx), which permit only error checking without error correction, this represents a significant improvement in system reliability.

Outlook

Through the introduction of the latest VLSI technology, VEB Microelectronics "Karl Marx" Erfurt is expanding and improving the available selection of newly coordinated components of the U80600 system. It is thus implementing a continuous concept of enhancement of the components based on the needs of the user industries and on the increasing requirements for future systems solutions.

Microprocessor U80601

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[Article by Andreas Fritzsche, VEB Microelectronics "Karl Marx" Erfurt, Research Center: "16-Bit Microprocessor U80601"]

[Text]

Foreword

The U80601 CPU is a modern efficient microprocessor with the potential for use in multiuser and multitasking systems. Depending on the application, the U80601 is up to six times more efficient than the CPU K1810 WM86, and the processor is downward compatible with the CPU K1810 WM86 from the software standpoint.

The U80601 permits two modes of operation: the direct address mode (real mode) and the virtual address mode (virtual protected mode or protected mode). Both modes of operation are programmable using the K1810 WM86 instruction set.

Real mode programs use a (directly addressable) address space of up to 1 MB, whereas in protected mode the U80601 automatically provides a virtual address space of up to 1 Gbyte per task, consisting of directly addressable blocks of 16 MB each.

Furthermore, protected mode provides memory protection, making it possible, for example, to separate the operating system from user programs and to process various tasks, involving both programming and data processing, at different privilege levels.

Both modes of operation use the same basic instruction set, registers, and addressing modes.

Assemblies of the U80601

As shown in the block diagram of the U80601 (Figure 1), the circuitry can be divided into the following assemblies:—Bus unit (BU)—Instruction unit (IU)—Execution unit (EU)—Address unit (AU).

Bus Unit

The bus unit contains address latches and drivers and the coprocessor interface as well as the data direction controller and bus controller for storage and I/O access of the U80601 and for coordination with coprocessors as well as bus allocation to master processors.

The unit uses the so-called prefetch mechanism, which looks ahead to the next instruction in a group of consecutive instructions. If a gap occurs within a sequence of

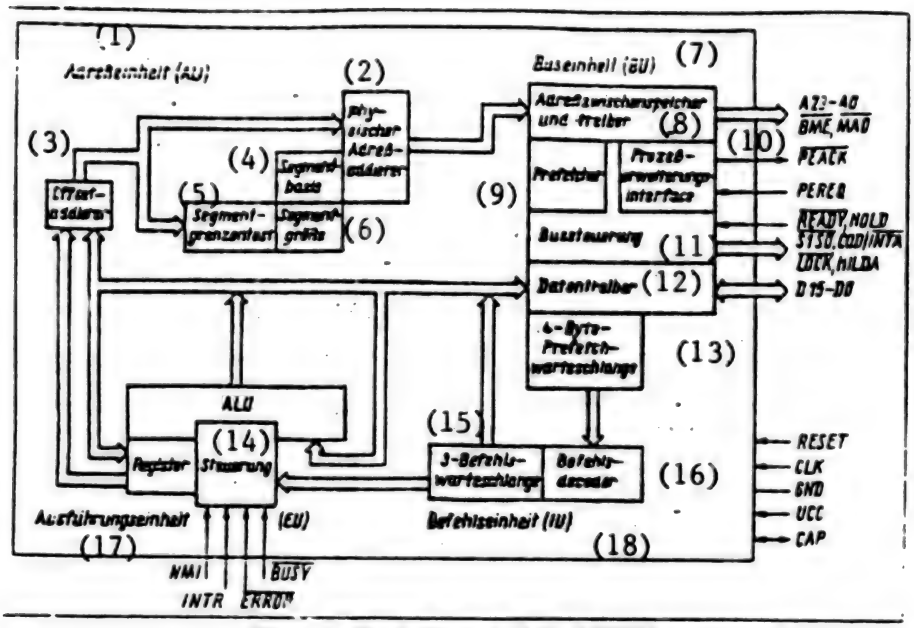


Figure 1. Block diagram of the U80601

Key: 1. Address unit (AU)— 2. Physical address adder— 3. Offset adder— 4. Segment base— 5. Segment limit check— 6. Segment size— 7. Bus unit (BU)— 8. Temporary address storage and driver— 9. Prefetcher— 10. Process expansion interface— 11. Bus controller— 12. Data driver— 13. 4-byte prefetch queue— 14. Controller— 15. 3 instruction queue— 16. Instruction decoder— 17. Execution unit (EU)— 18. Instruction unit (IU)—

instructions, the prefetch queue is reset to zero and the prefetch mechanism starts at the beginning of another sequence of instructions.

The 6-byte-deep prefetch queue contains instruction words not yet needed by the execution unit. This prevents idle times which occur with consecutive accesses to memory.

Instruction Unit

The instructions accepted by the prefetch queue are decoded by the instruction decoder of the instruction unit and placed in another queue which contains a maximum of three decoded instructions.

Execution Unit

Within the execution unit, the decoded instructions are taken from the queue and processed. This unit uses the bus unit for all data transfers from and to the memory or I/O port.

Address Unit

The address unit converts the virtual address into the physical address, as required by the bus unit, and checks, for each address, whether access is permissible and whether a segment limit has been exceeded.

Registers

The basic architecture of the U80601 includes 15 registers which may be classified into the four categories described below:

General Registers

Eight 16-bit multipurpose registers contain the arithmetic and logical operands, with four of these registers (AX, BX, CX, DX) able to accommodate either 16-bit operands or two separate 8-bit registers.

Segment Registers

Four special 16-bit registers permit direct access to four memory segments.

The segment registers are used to identify the four current segments, with each register assigned a specific type of segment:

- CS Code segment register
- DS Data segment register
- SS Stack segment register
- ES Extra segment register

The contents of these registers are called segment selectors.

Base Registers and Index Registers

Four of the general registers may be used to specify the offset addresses of the operands within memory. These registers may contain the base addresses or the index

(source index, object index) of the individual positions within the segments. The specification of this register, used for operand address computation, depends on the current addressing mode.

Status and Control Registers

Three special 16-bit registers contain the flag word, the instruction pointer, and the machine status word.

The 16-bit flag word contains special characteristics of the results of logical and arithmetical instructions (bits 0, 2, 4, 6, 7, and 8) and controls the operations of the U80601 within the given type of operation (bits 8 through 10).

The instruction pointer contains the relative address of the next instruction to be executed within the current segment. A 32-bit program counter can thus be determined in conjunction with the code segment register (CS).

The instruction pointer can be controlled implicitly with interrupt mechanisms, jumps, and control transfers. In the U80601, only the four low bits are used for the 16-bit machine status word.

Storage Organization

The storage of the U80601 is organized as a set of variable length segments. Each of these segments includes a linearly addressable memory area of up to 64 K. Addressing of memory is accomplished using a two component address. The components are pointers that contain a 16-bit segment selector and a 16-bit offset. The segment selector refers to the targeted storage segment while the offset component identifies the targeted byte address within the segment. All instructions which address operands within the memory must therefore specify the segment and the offset. In rapid and compact instruction processing, the segment selector is usually placed in the high-speed segment register. In this case, the instruction need only specify the targeted segment register and the offset to address the operands in the memory. However, with most instructions, it is not necessary to specify the required segment register explicitly because the correct segment register is automatically selected (according to fixed rules).

With prefixes which exceed the segment limits, it is possible to override the implicit segment register selection rules for special cases. With these, the stack, data, and extra segments may be identical to those of simple programs. A full 32-bit pointer or a new segment selector must be loaded to permit access to operands not contained in one of the segments directly accessible to the four segment registers.

Input/Output Area

The I/O area of the U80601 consists of 64 K 8-bit ports or 32 K 16-bit ports. I/O instructions address the I/O area either with an 8-bit port address which is specified in the instruction or with a 16-bit port address from the DX register. 8-bit port addresses are filled in with zeros so addresses A15 through A8 are low. I/O port addresses 00F8H to 00FFH are reserved.

U80601 Interrupts

An interrupt breaks off current program processing; the processor then resumes processing at a different location. The old program addresses (CS:IP) and the machine status (flags) are saved in the stack and thus permit a return to the interrupted program. Interrupts may be divided into three categories:—Hardware interrupts ;—INT-instructions;—Instruction exceptions.

Hardware interrupts are triggered in connection with the state of an external input and may be processed as masked or nonmasked interrupts. With an INT instruction, an interrupt may be triggered from a program. Instruction exceptions are activated when, in the attempt to process an instruction, abnormal conditions preventing further processing of the instruction occur. The return address of an exception always refers to the instruction which caused the exception and includes the preceding instruction prefixes.

A table may define as many as 256 pointers which contain special interrupt service routines for each interrupt. Interrupts 0 through 31, some of which are used for instruction exceptions, are already allocated.

With each interrupt, an 8-bit interrupt vector identifying a specific entry point must be sent to the U80601. INT instructions contain or implement this vector and have access to all 256 interrupts. Masked hardware interrupts deliver the 8-bit vector to the CPU during the interrupt acknowledge bus sequence. Nonmasked hardware interrupts use an internally delivered, predefined vector.

Maskable Interrupt (INTR)

The U80601 has a maskable hardware interrupt request input (INTR). By setting the interrupt flag bit (IF) in the flag word, this input may be released (IF = 1) or blocked (IF = 0) by the software. All 224 user-definable interrupt sources may use this input, with each of these sources able to have its own separate interrupt handler.

During the interrupt acknowledge sequence, the CPU reads an 8-bit vector by which the source of the interrupt may be identified. Within the servicing of the interrupt, the IF bit is reset as part of the response to the interrupt or the exception, and, consequently, additional maskable interrupts are blocked. The flag word saved in the stack contains the status (of the processor) in effect before the interrupt. The interrupt flag remains set on 0 until the flag word is written back into the flag register. The interrupt return [IRET] instruction includes, among other things, the restoring of the flag word and thus the restoring of the original status.

Nonmaskable Interrupt (NMI)

The U80601 also has a nonmaskable interrupt input (NMI). The NMI has higher priority than the INTR. A

typical use of the NMI is the activation of an efficient error routine. If the NMI input is activated, an interrupt is triggered by the internally delivered vector value 2. An interrupt acknowledge sequence is not activated.

While the U80601 executes the NMI service procedure, no additional NMI requests, no INTR requests, and no interrupt requests resulting from exceeding the coprocessor segment are serviced. If another NMI occurs while one NMI service routine is already running, this is acknowledged by the CPU and the NMI is processed after execution of the first IRET instruction. The interrupt flag bit (IF) is reset at the beginning of an NMI (IF = 0) to prevent masked interrupts.

Single-Step Interrupt

The U80601 has an internal interrupt which permits it to process programs in single-step mode (instruction by instruction). This interrupt is called the single-step interrupt and is controlled via the single-step flag bit (TF) of the flag word. Once this bit is set, a single-step interrupt is triggered after the execution of the next instruction. This interrupt uses an internally delivered vector with the value 1 and resets the TF bit. The IRET instruction is used to set the TF bit and to control the single-step processing of the next instruction.

Interrupt Priorities

Different interrupts occurring simultaneously are processed according to the following priorities:

Priority	Type of Interrupt
high	Instruction exception
	Single step
to	NMI
	Coprocessor segment overrun
	INTR
low	INT instruction

Interrupt processing includes, among other things, saving the stack and the return address as well as setting the CS:IP to the first instruction of the interrupt handler.

Real Mode

In the real mode, the U80601 is downward compatible with the K1810 WM86 instruction set. In this mode of operation, the U80601 is object-code compatible with software created using the K1810 WM86 processor. The physical memory of the U80601 consists of a continuous area of a maximum of 1 MB, addressed via address pins A0 through A19 and the BHE signal. Addresses A20 through A23 are ignored.

In the real mode, a physical memory of up to 1 MB is addressable via addresses A0 to A19. For this, an address is made up of two components: a segment selector and an offset component.

The 16 upper bits of a 20-bit segment address are interpreted as a segment selector. The four low bits of this segment address are always 0. Consequently, segment addresses are always multiples of 16 bytes. The offset component is composed of the 16 low bits of the offset address. The 4 upper bits of this address are 0.

In the real mode, all segments have a size of 64 K. Their content is readable, writable, and executable. If data operands or instructions attempt to access beyond the end of a segment (for example, a word with the low offset byte FFFFH and the upper offset byte 0000H), an interrupt or an exception may be triggered.

In the real mode, the U80601 reserves two fixed storage areas: the system initialization zone and the interrupt table zone. Storage locations with the addresses FFFF0H through FFFFFH are reserved for system initialization. Execution of initialization begins therefore with the address FFFF0H.

The memory locations of addresses 00000H through 003FFH are reserved for the interrupt vectors.

Protected Mode

In the protected mode (virtual protected mode), the U80601 is downward compatible with the K1810 WM86 instruction set. Furthermore, in the protected mode, efficient memory management is possible and a protection mechanism linked to specific instructions is activated.

With the setting of the PE bit (protection enable) of the machine status word using the LSMW instruction (load machine status word), the 80601 is switched from the real mode into the protected mode. The protected mode offers an expanded physical memory address space and a virtual memory address space, a memory protection mechanism, and new operations to support the operating system and the virtual memory.

Programs of the K1810 WM86 and programs generated in the real mode of the U80601 may be executed in the protected mode; however, they must be embedded in the various constants of the segment selectors.

Memory Space and Memory Addressing

In the protected mode, the U80601 has available a virtual address space of 1 Gbyte per task, which is partitioned into physically addressable blocks of 16 MB each and is addressed via address pins A23 through A0 and BHE. In the protected mode, as in the real mode, addressing is carried out using a 32-bit pointer consisting of one 16-bit selector component and one offset component. However, in this case the selector is not the 16 upper bits of a real memory address, but specifies the index of tables within the memory. The 24-bit base address of the targeted segment is created using this table. To determine the physical address, the 16-bit offset is added to the segment base address. As soon as a segment register is loaded with a selector, the tables are

automatically addressed by the CPU. All instructions of the U80601 that load segment registers access the tables in the memory without additional software. These tables, called descriptor tables, contain 8 bytes each.

Descriptors

Descriptors specify the use of the memory. Gate descriptors also specify behavior during task switching operations. The U80601 has descriptors for code, stack, and data segments and system descriptors for system data segments and control transfer operations. Descriptor accesses are executed as locked bus operations so descriptors may also be integrated into multiprocessor systems.

Code and Data Segment Descriptors (S = 1)

In addition to the segment base address and the segment length defined by the segment limit, code and data segment descriptors contain an access right byte which also contains attributes of the segment. This byte contains five pieces of information:

- Presence bit: The P-bit indicates the presence, i.e., the availability, of the segment.
- Descriptor privilege level: These two bits contain the privilege level of the selector.
- Accessed bit: The A-bit signals whether the segment has already been accessed.
- Segment descriptor: For code and data segment descriptors, the S-bit is always 1.
- Type: Three additional type bits contain further information depending on whether the descriptor is a code descriptor or a data segment descriptor.

Data segment: A data segment is identified by E = 0. The ED bit indicates the expansion direction of the segment, either in the direction of increasing or decreasing addresses. This distinguishes between stack and data areas. Another bit (W-bit) delivers information concerning the writability of the segment.

Code segment: For code segments, E = 1. The conforming bit (C-bit) is 1. Consequently, the code segment can only be executed if the current privilege level is not less than the descriptor privilege level and remains unchanged.

System Segment Descriptors (S = 0, Type = 1 Through 3)

System segment descriptors have a structure similar to code and data segments. These descriptors contain additional system information. The P-bit tells whether the segment is present in the physical storage or whether it is invalid. The type field specifies a valid task status segment (type = 1), a local descriptor table (type = 2), or an allocated task status segment (type = 3).

Gate Descriptors (S = 0, Type = 4 Through 7)

Gates are used to control access to entry points within an object code element. Depending on how this access occurs, a distinction is made between call gates, task gates, interrupt gates, and trap gates. The gates are defined in the type field. Gate descriptors also contain the object selector and the object offset.

The gates deliver the transfer level of a control transfer from the source to the object. The transfers permit the CPU to make automatic protection checks and to control the entry point of the object. Call gates are used to change the privilege level. Task gates are used to execute task switches. Interrupt and trap gates permit specification of interrupt service routines.

In contrast to the trap gate, the interrupt gate may block interrupts (by resetting IF).

Local and Global Descriptor Tables

The U80601 has two descriptor tables containing all descriptors accessible to a task at any time. A descriptor table consists of a linear array with up to 8,192 descriptors. The 13 upper bits of the selector value contain the index within a descriptor table. Each table has a 24-bit base register to locate the descriptor table in the physical memory and a 16-bit limit register which restricts descriptor access to a defined limit (Figure 2).

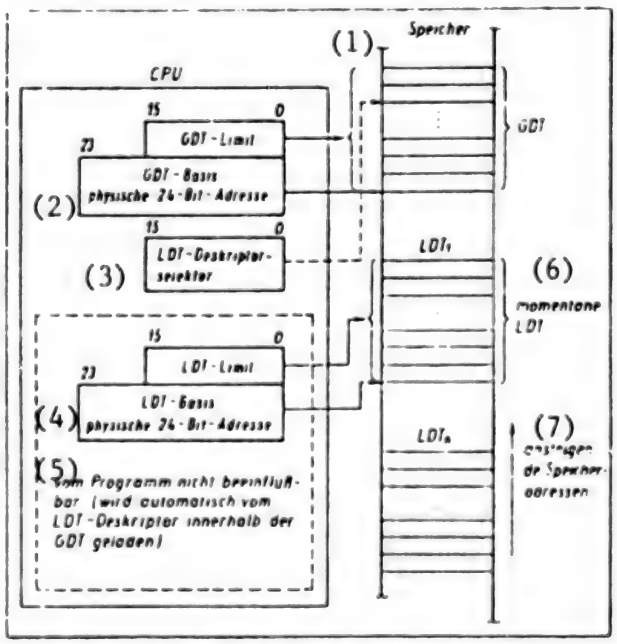


Figure 2. Local and global descriptor tables

Key: 1. Memory— 2. GDT base, physical 24-bit address— 3. LDT descriptor selector— 4. LDT base, physical 24-bit address— 5. Cannot be affected by the program (is loaded automatically by the LDT descriptor within the GDT)— 6. Current LDT— 7. Increasing memory addresses—.

One of the tables, the global descriptor table (GDT), contains descriptors available for all tasks. The second table, the local descriptor table (LDT), contains descriptors that may be used privately (locally) by the tasks. Each task may have its own local descriptor table.

The GDT may contain, in addition to interrupt and trap descriptors, all descriptor types whereas the LDT may contain only segment, task gate, and call gate descriptors.

If the segment descriptor does not exist in one of these two tables at the time of access to a task in this segment, this segment cannot be accessed by the task.

With the instructions LGDT and LLDT (LOAD GDT/LDT), the base and limit of the global and the local descriptor tables are loaded. The LGDT instruction and the LLDT instruction are privileged, i.e., they may only be executed from authorized programs which operate in privilege level 0. The LGDT instruction loads a 6-byte-long field that contains the 16-bit table limit and the physical 24-bit base address of the global descriptor table. The LDT instruction loads a selector that indicates a descriptor of the local descriptor table that in turn contains the base address and the limit of an LDT.

Interrupt Descriptor Table

In the protected mode, the U80601 has a third descriptor table, the interrupt descriptor table (IDT), through which it is possible to define 256 interrupts. This table may contain only task gates, interrupt gates, and trap gates. The interrupt descriptor table has available within the CPU a physical 24-bit base register and a 16-bit limit register. The privileged LIDT instruction loads this register with a 6-byte value, analogously to the LGDT instruction.

Access to the interrupt descriptor table may occur via INT instructions, external interrupt vectors, and exceptions which refer to this table.

The IDT must include at least 256 consecutive bytes to be able to allocate space to all reserved interrupts.

Privileges

The U80601 has a four-level privilege system which controls the use of privileged instructions as well as access to descriptors and the related segments within a task. This four-level privilege system represents an expansion of the user/supervisor mode frequently found in minicomputers.

The privilege levels are numbered from 0 to 3, with 0 representing the highest privilege level. The privilege levels permit protection within the task. Because private (local) descriptor tables are provided for each task, the tasks are isolated from each other. Operating system routines, interrupt handlers, and other systems software may be linked in the virtual address space to each task which uses the four privilege levels and protected. Each task of the system has a separate stack for each of its privilege levels.

Tasks, descriptors, and selectors have a privilege level attribute which specifies whether the descriptor may be used or not. Task privileges result in the use of instructions and descriptors. Descriptor and selector privileges result only in access to the descriptor.

Protection Mechanism

The U80601 has an extensive mechanism for protection of critical instructions which may affect the execution status of the CPU (e.g., HLT) and which protect the code or data segment from inappropriate types of processing. This protection mechanism includes three categories:

- restricted processing of the segment (e.g., write-protect for read-only data segments); the descriptors in the local descriptor table (LDT) and in the global descriptor table (GDT), define the availability of the segments for use.
- restricted access to the segments through the privilege rules and descriptor processing
- privileged instructions or operations which may be executed only in specified privilege levels and which are defined through the CPL and the I/O privilege level (IOPL); the IOPL is defined by bits 14 and 13 of the flag word.

The checks associated with the protection mechanism, executed with all instructions, may be classified into three groups:

- Segment load checks
- Operand reference checks
- Privileged instruction checks.

If execution of the check detects a processing rule violation, an exception is triggered, permitting reaction to this violation.

System Interface

The system interface of the U80601 may be set up as a local bus and as a system bus. The local bus consists of address, data, status, and control signals of the U80601. A system bus is a buffered version of the local bus.

The U80601 family includes different assemblies with which it is possible to set up a standard bus system such as the modular microcomputer system MMS 16.

The microsystem local bus interface communicates with local memory and I/O components of the U80601. This interface consists of 24 address signals, 16 data signals, and 8 status and control signals.

A system bus may be made up, for example, of the components CPU (U80601), pulse generator (DS82284), bus controller (U80606), bus arbiter (80609) as well as bus driver (DS8286/8287) and latches (DS8282/8283).

The pulse generator DS82284 generates the system pulse and synchronizes READY and RESET. The bus controller U80606 converts the decoded bus operation

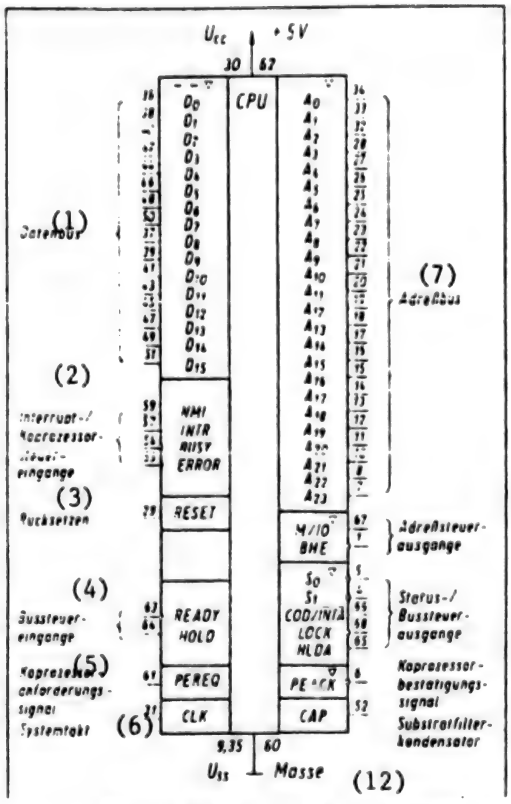


Figure 3. Diagram of the U80601

Key: 1. Data bus— 2. Interrupt/coprocessor control inputs— 3. Reset— 4. Bus control inputs— 5. Coprocessor request signal— 6. System pulse— 7. Address bus— 8. Address control outputs— 9. Status/bus control outputs— 10. Coprocessor acknowledge signal— 11. Substrate filter capacitor— 12. Ground

status into command and bus control signals. The bus arbiter U80609 generates MMS-16-bus-oriented signals.

These components deliver the required time relationships, the electrical levels, and the driver output for most of the system bus interfaces including the MMS 16.

Bus Operation

The U80601 uses a system pulse with double frequency (CLK input) to control bus timing. All local bus signals are derived relatively from this system pulse input. To generate the internal processor pulse, which determines bus status, the system pulse is divided in two. A processor pulse consists of two system pulse cycles, called phase 1 and phase 2.

The CPU supports six types of bus operations:

- Memory read operation
- Memory write operation
- I/O read operation
- I/O write operation
- Interrupt acknowledge operation
- Halt/Shutdown operation.

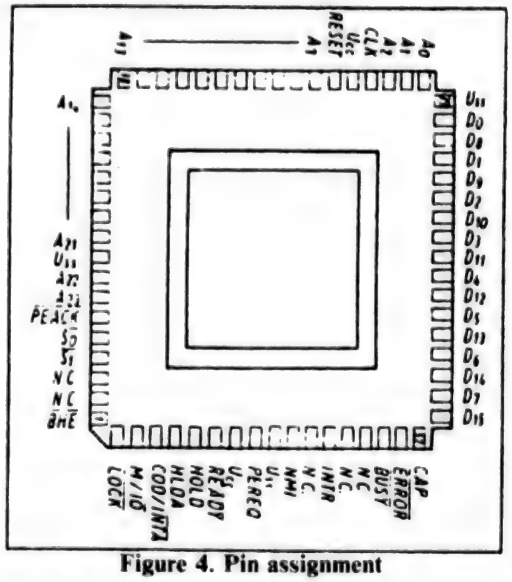


Figure 4. Pin assignment

During data transfer a maximum of one word may be transferred within two processor pulse cycles.

The U80601 has three basic states:

- Idle (Ti)
- Send status (Ts)
- Execute command (Tc).

A fourth local bus state of the CPU is called halt (Th). The Th state indicates that the U80601 has transferred control of the local bus to another bus master in response to a HOLD request.

The idle state indicates that no data transfer is taking place or requested. The first active state Ts is signaled by setting the status signals S1 and/or S2 on low. This identifies phase 1 of the processor pulse. During Ts, the command is decoded, and the addresses and data (in write operations) are released. The bus controller U80606 decodes the status signal and generates MMS-16-bus-compatible read or write commands as well as the control signals of the local driver.

Following the state Ts, the command execution state Tc is assumed. Storage or I/O systems react to this bus operation within Tc by either transferring read data to the CPU or accepting write data. To assure adequate reaction time of the storage or I/O systems, the Tc state is repeated as often as necessary. The READY signal indicates whether Tc is repeated or not.

A repeated Tc state is called a WAIT state. During the halt state (Th), all address, data, and output pins of the U80601 are highly resistive to permit a different bus master to use the local bus. The HOLD input signal is used to set the U80601 in the Th state. The HLDA output signal indicates that the CPU has assumed the Th state.

Summary

The U80601 is a fast 16-bit microprocessor developed for use in efficient personal computers and automatic control devices. For this, the U80601 meets international PC standard specifications.

The U80601 is distinguished by a high operating speed (pulse frequency up to 16 MHz) with increased data throughput (pipelining, prefetching) and a large address space (one gigabyte per task).

To assure development and production of a new efficient generation of personal computers, the U80601 offers a CPU which corresponds to the latest international requirements (potential for use in research, development, design, process control, etc.).

[Box, p 135] Pin Description of the U80601 (I = Input; O = Output)

Symbol: BHE; Pin: 1; I/O: O

Function: Byte High Enable (low-active) is activated during data transfers on the high byte of the data bus D8 through D15. 8-bit systems, to which the higher data byte is normally directed, may be selected using the BHE signal.

The signal is highly resistive during bus hold acknowledge.

Transfer Capabilities:

BHE	I0	Function
0	0	Word transfer
0	1	Byte transfer of high data byte
1	0	Byte transfer of low data byte
1	1	Not used

Symbol: S1, S0; Pin: 4, 5; I/O: O

Function: Bus Status (low-active) signals activity of the bus and, together with the signals M/IO and COD/INTA, makes it possible to determine the bus cycle type. Signals are highly resistive during bus hold acknowledge.

Bus Status Definition

COD/ INTA	M/IO	S1	S0	Bus cycle
0	0	0	0	Interrupt acknowledge
0	0	0	1	Not used
0	0	1	0	Not used
0	1	0	0	If A1 = 1, then halt, otherwise shut down
0	1	0	1	Read storage data
0	1	1	0	Write storage data
1	0	0	0	Not used
1	0	0	1	Read I/O
1	0	1	0	Write I/O
1	1	0	0	Not used
1	1	0	1	Read storage instruction
1	1	1	0	Not used
x	x	1	1	No bus cycle

Symbol: PEREQ, Pin: 6, I/O: I; PEACK, Pin: 6, I/O: O

Function: Processor Extension Operand Request and Acknowledge (PEREQ—high-active, PEACK—low-active) expands the memory management and protection capabilities of the U80601 for the use of coprocessors. The PEREQ input signal permits the U80601 to initiate a data operation transfer to the coprocessor; the PEACK output signal informs the coprocessor of the transfer of the requested operand. PEACK is asynchronous to the system pulse. PEREQ is highly resistive during bus hold acknowledge.

Symbol: A23 through A0; Pin: 7 through 34; I/O: O

Function: Address Bus (high-active). Signals for output of physical and I/O port addresses. A0 is low with data transfer of pins D7 through D0. A23 through A10 are low during I/O transfers. The address bus is highly resistive during bus hold acknowledge.

Symbol: RESET; Pin: 29; I/O: I

Function: System Reset (high-active) resets the internal logic of the U80601. The U80601 may be initialized at any time after a high-low impulse and activation of the RESET input (halts on high) of at least 16 system pulse periods. While RESET is active, the output pins of the U80601 are assigned the following logical states:

Pin state	Pin designation
1 (high)	S0, S1, PEACK, A23-A0, BHE, LOCK
0 (low)	M/IO, COD/INTA, HLDA
highly resistive	D15-D0

The U80601 starts its operations after the high-low impulse on RESET. This impulse must be synchronized with the system pulse. Approximately 50 system pulses are required for the internal initialization of the U80601 before the first bus cycle for acceptance of the code from the power-on start address can occur. A low-high impulse on RESET, synchronized with the system pulse terminates a processor cycle with the second high-low impulse of the system pulse. If the high-low impulse is asynchronous to the system pulse, it is impossible to determine which phase of the processor pulse is present during the

next system pulse period. Low-high impulses synchronous to the system pulse are required only for systems in which the processor pulse must be phase-synchronized with another pulse.

Symbol: CLK; Pin: 31; I/O: I

Function: System Clock generates the basic timing for U80600 systems. The U80601 divides this pulse in two to generate the processor pulse internally. The divided pulse may be synchronized by an external pulse generator through a high-low impulse to the RESET input.

Symbol: D15 through D0; Pin: 36 through 51; I/O: I or O

Function: Data Bus (low-active). Data inputs during storage, I/O and interrupt acknowledge read cycles. Data outputs during storage and I/O write cycles. The data bus is highly resistive during bus hold acknowledge.

Symbol: BUSY, ERROR; Pin: 53,54; I/O: I

Function: Processor Extension Busy and Error (low-active) indicates the operating state of a coprocessor. An active BUSY input prevents the execution of WAIT instructions and some ESCape instructions until BUSY is inactive (high) again. The U80601 may be interrupted while waiting for an inactive BUSY. An active ERROR input signals coprocessor errors and permits the U80601 to trigger an interrupt (interrupt 7) upon additional execution of WAIT or ESCape instructions.

Symbol: INTR; Pin: 57; I/O: I

Function: Interrupt Request (high-active) permits interruption of a running program and the jump to an interrupt service routine. Interrupt requests are blocked as long as the interrupt enable bit of the status register is set on 0. After the U80601 has accepted an interrupt, it generates two interrupt acknowledge bus cycles to read an 8-bit interrupt vector and to detect the source of the interrupt.

At the start of an interrupt program, INTR must remain active until the end of the first interrupt acknowledge cycle. The INTR input is queried at the beginning of each processor cycle and must be high for two processor pulse periods before the end of the current instruction so the interrupt is accepted before the next instruction. The INTR input is power-level sensitive and may be activated asynchronously to the system pulse.

Symbol: NMI; Pin: 59; I/O: I

Function: Nonmaskable Interrupt Request (high-active) interrupts the U80601 with the internal generation of an interrupt vector (interrupt 2). No interrupt acknowledge cycles are triggered. The interrupt enable bit is not evaluated. For detection of an NMI, the signal must be inactive (low) for at least four pulse periods, then be set to high, and hold this active state for four additional pulse periods. The NMI input is impulse-sensitive, and the interrupt may occur asynchronously to the system pulse.

Symbol: READY; Pin: 63; I/O: I

Function: Bus Ready (low-active) indicates the end of a bus cycle. Bus cycles may be generated continuously until they are terminated with low on the READY signal. During bus hold acknowledge, the signal is ignored.

Symbol: HOLD, HLDA; Pin: 64; I/O: I or O

Function: Bus Hold Request and Hold Acknowledge (high-active) determine the control of the U80601 local bus. The HOLD input permits other masters to request control of the local bus. If the bus control can be transferred to other masters, the bus drivers float in the highly resistive state, the HLDA signal is activated, and the U80601 assumes the bus hold acknowledge state. If the hold signal is inactive, the U80601 can resume local bus control whereby the HLDA signal is reset and the bus hold acknowledge state terminated. Activation of the HOLD input can occur asynchronously to the system pulse.

Symbol: COD/INTA; Pin: 66; I/O: O

Function: Code/Interrupt Acknowledge. Signal to acknowledge instruction-fetch-cycles or storage data read cycles or I/O cycles. COD/INTA is highly resistive during bus hold acknowledge.

Symbol: M/IO; Pin: 67; I/O: O

Function: Memory I/O Select. Signal for separation of memory and I/O cycles. If the signal is high during the status cycle (Ts), this indicates a memory cycle or a halt or shutdown. A low level indicates an I/O cycle or an interrupt acknowledge cycle. The signal is highly resistive during bus hold acknowledge.

Symbol: LOCK; Pin: 68; I/O: O

Function: Bus Lock (low-active) prevents other system bus masters from assuming control of the bus within the next bus cycle. The signal can be activated using the LOCK instruction and is automatically activated during the execution of the XCHG instruction (eXCHanGe register-storage or register accumulator), within the interrupt acknowledge cycles (guarantees two consecutive cycles for INTA), and during access to descriptor tables. LOCK is highly resistive during bus hold acknowledge.

Symbol: Vcc; Pin: 30, 62; I/O:—Function: Operating voltage +5V

Symbol: Vss; Pin: 9, 35, 60; I/O:—Function: Ground

Symbol: CAP; Pin: 52; I/O: I

Function: Substrate filter capacitor. Between this pin 52 and the ground, a capacitor 47 nF +/-20 percent, 12 V must be connected. This capacitor serves to equalize possible voltage surges.

GDR's IMAGE-C Software Applied to Image Processing

23020068 East Berlin NEUE TECHNIK IM BUERO in German May-Jun 89 pp 93-96

[Article by Detlef Gebhardt of Robotron Marketing VEB, Berlin: "Image Processing Based on the PC With the IMAGE-C (DCP/C) Software System"]

[Text]

Demands on Image Processing

In comparison with other areas of information processing, image processing has a few special characteristics:

1. Large amounts of data must be analyzed and reduced to the share of information essential from the user's perspective, meaning at least some parts of an image processing system must work extremely fast and efficiently.

2. A broad spectrum of information processing problems are directly or indirectly affected: a. simple numerics, statistical analyses, transformations, filters; b. topological and metric structural analyses; c. adaptive algorithms, such as classifiers, data banks and expert systems. This means that an image processing system should be open to all sides and enable the integration of further-reaching software.

3. There is generally no closed theory for the immediate solution of specialized analysis tasks, but rather partial solutions, which must be selected, adapted and put together in a suitable manner. This means that a programming language and environment are needed, which support an effective heuristic search for a suitable algorithm or a suitable technology, respectively.

For about 6 years the Robotron VEB combine has developed and operated image processing systems and corresponding user software in cooperation with the Academy of Sciences of the GDR and other institutes.

The computer-technological basis for this has up to now been the 16-bit K 1630 minicomputer with image-processing-specific peripherals for sequential (BVS A 6471) and parallel (BVS A 6472/73) processing.[1] Experience from using the IPU, DIXI and AMBA software systems or user packages, for example in remote sensing, medicine and materials science, evaluation of international trends as well as the anticipated developments in hardware, impose the following demands on the new development of image processing systems:

1. Workplace-related, decentralized image processing based on 16-bit PCs with powerful special periphery.

2. Networked, decentralized work stations via LAN with preprocessing centers and data banks, centered around a 32-bit minicomputer, for example.

3. General, menu- or command-controlled image processing software for direct utilization by professionals without knowledge of programming.

4. Modification and production of programs as well as program runs with the help of expert systems as program generators for non-programming professionals.

5. Subprogram libraries for modular solution of tasks for expert systems or by professionals with certain programming knowledge.

6. Possibilities for programming specific image processing or evaluation functions in a multitude of common standard languages.

7. Portable image processing software, which is also implementable on new hardware solutions at little expense, an open system which enables expansion and adaptation and encourages standardization in the exchange of programs and knowledge by the users on the basis of commercially distributed systems software and programming languages.

Application Area

Due to the widespread use of personal computers, the number of users who are interested in the solution of image processing tasks is also growing. Thus, the number of potential applications is also reaching a new level. The focal point of the IMAGE-C software system was aimed at image analysis and image interpretation. High-capacity modules are therefore available for segmenting, measuring and classifying individual objects or regions and for acquisition of their relationships in the image. Interactive image manipulation, such as is the precondition for many visual interpretive tasks, also becomes possible.

The flexibility as well as expandability and openness of the IMAGE-C library thus makes it possible to cover a wide field of applications. Among the essential application areas are, for example:

—Medicine and biology (histology, chromosome analysis, biocatalyst research, ophthalmology)
—Materials research (structural analysis of raw materials, construction materials and materials in: a. metallography; b. ceramography; c. plastography; d. mineralogy, e. petrography; f. evaluation of nuclear track detectors
—Remote sensing of the earth (agriculture and forestry, cartography, geology, environmental protection...)
—Astronomy (planetary and comet research)
—Industrial inspection (quality and status acquisition)
—Evaluation of image representation from special sensors (X-ray, microwave, infrared, ultrasound, isotope images)
—Training, for example at institutions of higher learning and technical schools.

Since there is scarcely a field in which people do not have to work and live with visual information, the application field for image processing is constantly expanding. Theoretical and experimental work on this is undertaken at academies, secondary schools and institutes. In this context this image processing system may serve as a development system for special solutions.

Hardware Requirements

On the hardware side the abovementioned demands are met with the production of the mini-image processor and the development of a new image processing system based on the personal computer, the BAS A 757x image analysis system. The work aimed at local networks and at the RVS K 1840 32-bit computer within the framework of the Robotron combine will also permit correspondingly centralized image processing system solutions after 1990.

Until the production of an image processor of the next generation (BAS A 757x), which represents a considerably improved concept on the basis of new technologies and components such as a graphics processor, the proven K 7067.15 graphics control, with a 16-bit PC will already create a noticeable modernization of the BVS A 6471. This graphics control, which in combination with the L 1630 has made image processing possible, is now connected to the EC 1834 16-bit PC with a special double card. The double card can be plugged into the EC 1834 or, in a special variant, into compatible PCs.

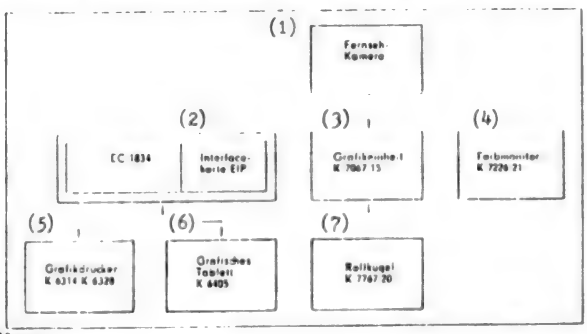
Once again, the most important parameters for the K 7067.15 graphics control:

- Video memory: 512 x 768 x 8 bit
- three palettes, 256 bytes each
- pixel and matrix access
- cursor overlay
- magnification 1...16
- text mask and
- video input for standard TV signal

Thus, a smaller and less expensive image processing system (Fig. 1) [not reproduced] compared to the BVS A 6471 can be utilized with comparable performance capability.

The standard variant of the mini-image processor, which is represented in Fig. 2, consists of:

The EC 1834 with a hard disk, EIP interface card, K 7067.15 graphics control, track ball unit, color monitor and K 6314 dot matrix printer, as well as a UFK 12 or TFK 1010 television camera.



Key:
1. TV camera
2. Interface card EIP
3. Graphics unit
4. Color monitor
5. Graphics printer
6. Graphics tablet
7. Track ball

In addition, it is useful to include a K 6405 graphics card for many applications.

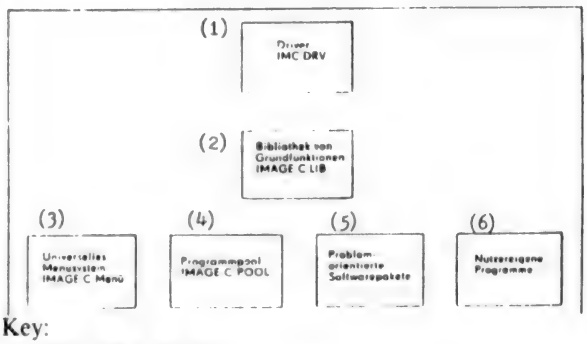
Organization of the IMAGE-C Software System

Basics of the Software System

The IMAGE-C image processing herewith presented is based on sequential processing of image-processing-specific functions or algorithms and represents an optimal conversion of the demands listed under 1 in connection with modern 16-bit PCs. The foundation is the DCP 3.2 operating system, which is fully compatible with the standard operating system for this class of equipment. The selection of programming language C as the implementation basis follows international trends and standards of modern software technology, and also offer the user the opportunity to write extremely efficient programs and to be able to use a broad spectrum of foreign programs.

High-capacity compiler packages exist, which offer an effective interactive development environment from editing to test. Beyond that, it is possible to use other languages such as PASCAL or FORTRAN. The C-programs are designed so that they can easily be adapted to other computer and operating systems. In designing the systems concept, the aspect of far-reaching portability was also taken into account by the fact that central, relatively small interfaces between software and hardware were foreseen.

An extensive library of function modules makes it possible to solve small image processing tasks rapidly, but it also becomes possible to master extensive projects in an elegant way, perhaps by including other software. Parts of the library can be directly addressed or entire groups of tasks be processed in a simple manner through a menu system. The components of IMAGE-C are shown in Fig. 3. This open concept meets the demands of for example Voss[2] for modern software technology. In particular to be mentioned are:



Key:
1. IMC-DRV driver
2. IMAGE-C LIB library of basic functions
3. Universal IMAGE-C Menu menu system
4. IMAGE-C POOL program pool
5. Problem-oriented software package
6. User-defined programs

Modularity:

A library of basic functions in the higher program language C is offered. These basic functions serve to solve elementary image processing tasks, and they can also be called up from programs written in PASCAL or FORTRAN. This library can be expanded by the user, whereby it is possible to build immediately on the given software.

Portability:

By using the C programming language the demand for portability of the worked-out programs to new hardware platforms is largely met. A precondition is the use of comparable graphics (sequential processing). Only the relatively small hardware interface must be adapted to the hardware factors.

Efficiency:

The demand for efficiency relates both to the expense of development and maintenance of programs and to the execution times. The selection of the standard C language for implementing the functions and programs satisfies both parts. On the one hand, creating a machine-oriented code assures rapid execution times, and on the other it offers the advantages of a high-performance development environment and of structured programming.

Complexity:

Based of the library of basic functions, complex solutions are offered for special application areas. By using the menu technique, the existing knowledge is processed in a user-friendly manner.

On the individual components:

The IMC-DRV driver forms the interface to the image-processing-specific hardware and represents the lowest level of the software system. The IMAGE-C library of basic functions is built on this driver. The elements of this library undertake elementary image processing steps, in order to arrive at complex solutions by combining these functions.

The upper level of the system, the user interface, operates on the basis of the latter two complexes—the driver and the library of basic functions. It includes a universal IMAGE-C MENU menu system as well as the IMAGE-C POOL program pool. All the components mentioned are included in the so-called IMAGE-C basic software package. In addition, user-oriented software packages, which are based on the basic software package, have been developed in cooperation with the research institutes of the GDR. One of the first is the IMAGE-C MATAN package. This package solves image-processing-specific tasks in materials research. It is developed by the Freiberg Mining Academy[4]. Additional packages will deal with applications in medicine, biology, for example chromosome analysis, or will enable the solution of problems in multi-image processing (IMAGE-C MIP).

In the following, primarily the components of the basic software package will be presented.

Components of the IMAGE-C Basic Software Package

Hardware Interfaces.

The IMC-DRV driver represents the lowest level of the software system. It contains those functions which make it possible to address the image-processing-specific hardware. Among them are, for example:

- Initializing of the EIP interface card
- reading and writing an individual point
- reading and writing a matrix
- programming the camera register
- loading palettes
- adjusting magnification
- setting cursor coordinates.

The driver is the only program part that is written in assembler language.

Library of Basic IMAGE-C LIB Functions

This library is relatively independent of hardware. When needed, it calls up the necessary driver functions. The library contains basic functions which are needed for carrying out image processing functions. They serve user groups which have available to them experts with programming knowledge, as a basis for programming their own application solutions. The groups of basic functions are listed, together with a few important functions, in the following:

Image input:—Visualizing and scanning a TV camera picture;—Accumulation of camera pictures;—Loading of an image on mass storage units

Image processing:—Graphics manipulation: a. setting the standard color tables; b. setting the global window; c. describing a matrix with a gray value d. modifying the cursor coordinates; e. setting the magnification

Image operations:—Image of window operations with the following functions: a. addition; b. subtraction; c.division; d. minimum, maximum; e.logical operations

Filters:—a. standard filters; b. optional filters

Geometric transformation: a. linear, quadratic and cubic image transformation; b. central projection

Image analysis:
—A. Object search and sentinel generation—1. object isolation; 2. determination of object sentinels; 3. slicing up object conglomerates;
—B. Gray value statistics in the image window
—C. Parallelepiped classification
—D. Hierarchical classification

—E. Voronoi decomposition and Delauney triangulation

Image output:—1. Storage of an image in a mass storage unit—2. Hard copy on printer

Statistical package:
—A. Random test analysis; Calculation of the sum of the entered values, the standard deviation and the slope
—B. Histogram analysis; Construction of histograms and output of these for random tests of optional sentinels
—C. Regression analysis; Construction of regression areas, classification of values and evaluation
—D. Statistical tests; 1. Kolmogorov-Smirnov test for agreement of distributions; 2. F-Test for equivalence of the variance of two normally distributed populations; 3. t-Test for agreement of the average values of normally distributed stochastic variables

Numerics package—Solution of some frequently occurring numerical problems, such as equation systems and calculation of eigenvalues and eigenvectors of symmetric matrices

Arithmetic operations, input functions

—Graphic functions: a. line production; b. character font loading; c. drawing a square

—Help functions: a. file search, open file; b. support of the graphics tablet.

The library is delivered in the form of a C object module library.

IMAGE-C-POOL Program Pool

For individual functions or for functions that belong together by context (histogram formation, object isolation) of a generally valid nature, programs are made available as source texts in a program pool. On the one hand these programs can be sensibly utilized for simple image manipulations—this manner of working resembles a command system—and on the other hand they have an illustrating character and clarify the handling of the library components.

In Fig. 4 [not reproduced] the menu of such a program named p-grahis for calculating the gray-value histogram of a randomly chosen window is shown. In the first step the window must be determined with respect to position and size.

Universal IMAGE-C MENU Menu System

IMAGE-C-MENU is the interactive user interface of the basic IMAGE-C software package. The program package has been realized as a window-oriented interactive menu system (pull-down menus).

This menu system is designed for universal application. It is primarily intended for users without programming knowledge. On the other hand, however, it is suitable for rapid testing of algorithms or technologies for image processing. In addition to the purely interactive work with IMAGE-C-MENU, it is possible for the user to define a series of interactively chosen functions as so-called macros as well as to store and process these macros. The user has thus been given a means to program within the menu system, without having to leave it and without using a special programming language.

IMAGE-C-MENU is based to a very high degree on basic functions of the IMAGE-C LIB library; by so doing, it is possible to convert algorithms or technologies tested with IMAGE-C MENU into rapid user programs in one of the possible programming languages without encountering problems. Fig. 5 [not reproduced] shows an example of a menu page. In the header of each page the chosen work mode can be seen (INTERAKTIV WORK, DEFINE MACRO or EXECUTE MACRO). On the left side of the main window the function selection windows are opened, nested within one another. This enables the user at all times to trace the chosen path. In the middle of the main window, a window for variable input is opened when necessary. This is supported by an integrated editor.

On the right side of the main window, parameters or sentinel indicator windows are opened. Through these, the user can obtain information about designated parameters or measured sentinels.

In the bottom line of a menu page the potentially available control over function keys is shown.

The menu system also supports work with a mouse to select the functions.

Summary

The IMAGE-C software system offers a system which enables effective image processing with 16-bit PCs. Special emphasis was placed on the development of practice-oriented elementary function modules and their time-optimal processing. Based on the basic package consisting of IMAGE-C LIB, POOL and MENU, user software packages are being developed for special applications.

IMAGE-C offers both professionals in special disciplines without programming knowledge and those with limited or extensive programming knowledge an optimal entry and the opportunity for problem-oriented, independent, in-depth solution of image processing tasks.

Furthermore, because of the selection of the C language and the IMAGE-C concept, rapid conversion of the system without loss of efficiency to PC image processing systems with expanded image processing hardware has become possible. IMAGE-C therefore becomes the basic system for a new generation of image processing systems by the Robotron combine. In addition to the software system, Robotron offers know-how in the solution of tasks involving image processing, implementation, support and training.

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Czech Views on Distributed Data Processing Problems, Limitations

24020022 Prague MECHANIZACE A AUTOMATIZACE ADMINISTRATIVY in CzechNo 4, 1989 pp 121-124

[Article by Vaclav Chvalovsky, CSc, PZO KOVO, Prague: "Problems and Limitations of Distributed Data Processing]

[Text]

Inspiration and Motivation

The following paragraphs will probably be like adding "oil to fire." The "fire" represents continuing discussions about microcomputers, and in particular, personal computers. We note these discussions not onlyamong our specialists but among those for whom, until recently, thecomputer was nothing but a diabolic implement of destruction. Because the basic terms microcomputer and personal computer are sufficiently known, we will not waste time with definitions.

This article was inspired by a large number of other articles,presentations and similar reports dealing with the subject of using microcomputers and personal computers in our economy and elsewhere: some of these were written by the author of this article. In order to more readily assess the value of the thoughts embodied in these articles, they are listed at the top of the list of references numbers [1] through [3]. A great number of specialists have expressed an opinion on this subject. They have to be credited with a great amount of inventiveness and a contribution to the clarification of the role of these computer devices in the automated data processing in our economy. Articles which have interested the author the most are items [1] through [7]. However-,there must certainly be many more. Most of these articles have one thing in common and that is that they were written in an era which can be called "fledgling" in terms of a broader or even a mass application of this class of computer technology in our economy. In spite of the fact that we still cannot speak of significant progress in this sector (mass use), we are, however, much richer in experience. The intention of the author of this article is to compare the present conceptions and expectations as expressed in the literature on the subject of micro/personal computers with the present-day experiences involving the use of these computers at various locations. As a base for this article, we will use the author's own place of business; but,the facts obtained should be universal. This is confirmed by conclusions from many conversations and consultations with other organizations and institutions throughout the CSSR.We will try to focus on a route that will lead from a "youthful enthusiasm" towards restrained and objective evaluation of reality.

Expectation Versus Reality

(Problems With the Use of Micro/PersonalComputers)

As an introduction, let us make a short terminological comment. Abroad,it is customary to mention distributed data processing in the same breath as the use of micro and personal computers. We will do the same. Problems associated with the introduction and application of this category of computer technology will be considered identical to the problems with distributed data processing. However, purely theoretically, they are in fact not identical. Distributed data processing is also a problem in terms of the use of a mainframe. In the following text we will present the most often described and emphasized advantages of using this category of computer technology—in literature as well as in practice—and compare them to today's reality (claim versus reality).

Claim I: "Micro/personal computers will be used extensively, at practically all work sites responsible for data processing...."

The reader need not worry. We will not waste our time with useless discussions on the subject of accessibility/nonaccessibility of these computers in our economy. We will only state that the pessimistic evaluation of our reality has practically not changed in the last 2 years. There is nothing left to do but hope that the present extensive rearrangement of capacities and the integration of economic activities into one area will contribute to the improvement in this area. In spite of an insufficient amount of technical means (better yet:thanks to this insufficiency—a paradox), one of the tenets of the cited inspirational sources has been corroborated. It is totally obvious that to consider the use of distributed data processing makes some sense only if we equip all centers of the information system with a sufficient number of terminals for micro- or personal computers or

with personal computers themselves. To make it perfectly clear—Even though, so far we do not know to what extent work productivity improves with the introduction of these types of computers, it is apparent that we cannot accept a situation where the users of the computers must wait for the use of a terminal. If we ignore serious negative psychological effects we waste valuable human initiative. Not everyone will agree but it is a fact that there is agreat difference between using a mainframe terminal and using a terminal on a personal computer. The quickly acquired feeling of "owning" apersonal computer creates a feeling that this ownership is applicable towards good use. To deny that has negative consequences.

Claim II: "A microcomputer or a personal computer makes it possible to adequately deal with more flexible automation goals than those encountered in the development of the Automated Control System...".This is undoubtedly the strongest motivation to install this technology. This is true in general and its significance is undisputed. Practical experience does, however, reveal some consequences which economic management does not accept without reservations. In simpler terms, wecould say that, by changing to a distributed data processing system with a system of connected personal computers, higher demands are placed on a perfect organization of automation.

What seems to be happening is that, when automation is understood in those terms, long-standing (and covered up) differences between the old-fashioned understanding of organizational management structure in our enterprises and institutions and the needs of automation are accentuated. Thus, the problems created can be divided into several areas:

1. The increased work productivity brought about by the use of personal computers reveals the reserves and sources of manpower savings. With very few exceptions, these manpower savings have been squandered through useless additional work. In other words, there is a lack of resolve with regard to this issue in purely economic terms, i.e., according to the principles of strict economic parsimony—i.e., profit/loss system of management.

2. At the moment micro- or personal computers are incorporated into the system, the instability of our organization structures will be revealed. On the outside, it seems to be a superficial problem. In the case of terminal computer networks, when there are work place or other organizational changes, it is enough to relocate the terminal. The personal computer network is a much more sensitive organism. Workers at computer centers with similar networks will confirm how difficult it is to maintain reliable connection between discrete elements by means of communication flowcharts or other expedients. It is a fact that even a slight change will necessitate a significant change in a system's parameters. The reason for that is that the distribution of the database within a network makes it necessary to fix the flow of data perturbed by organizational changes. Nevertheless, the fact remains that, until we are confronted with such issues, we are not able to appreciate fully the significance of fixed (and simple) organizational structures. Even though this claim does not apply equally to all micro-and personal computers, it is probable that only a more widespread application of the UNIX operational system can bring a solution to this problem (see continuation).

From the above it is apparent that, for achieving the desired results,the present standard of technical equipment for micro- and personal computers demands a much more stable organizational structure than has been the case in our automation system.

Claim III: "The best results using micro- and personal computers can be obtained by connecting them to the mainframe...." A broader application of data transfer and computer communication is precipitated by these connections. Our problems with these are wellknown and criticized. Connecting the micro- and personal computers to the mainframe [computer] of an organization/institution is in many cases directly dependent on the quality of connection. In local networks witha transfer rate of around 2 million characters per second (Microlan,etc.), then, in the case of external communications, the demands will be five times greater (Oslan, etc.). In other words, we are confronted with a totally unsolvable problem. Nevertheless, the experience at many work places has shown that, given our circumstances, we have insufficiently utilized the possibilities of indirect data transfer (off-line) between personal computers and the mainframe.The most common examples of such communications is the preprocessing and the so-called "post-processing" of data which are, after all, typical operations conducted on personal computers (in relation to the mainframe). Figure 1 represents one of the "off-line" solutions for data processing. The expedient applied is a magnetic tape transferred between the microcomputers and the mainframe, in both directions. Practical experience with this has been consistently positive.

Claim IV: "Micro- and personal computers offer possibilities of extensive use in the economy, beginning with automated text processing and ending with applied programming...".Experience will probably support the following claims based on utilization. As we all know, advertisement slogans do not always tally with the facts. The areas of use will be ordered in terms of desirable procedures in utilizing micro- and personal computers, which follow a general rule, i.e., going from the most simple to the most complex (the most common to the most specific):

1. Automated data processing is generally considered to be an unusually effective utilization of personal computers (see for example [2] and [6]). It is known that, abroad, specialized computers with corresponding programs are manufactured for this purpose. Their price has approached that of electric typewriters. Justifiably, the conclusion is drawn that the future of typewriters is nil because work productivity, when using micro- and personal computers, is two and a half times greater. Under

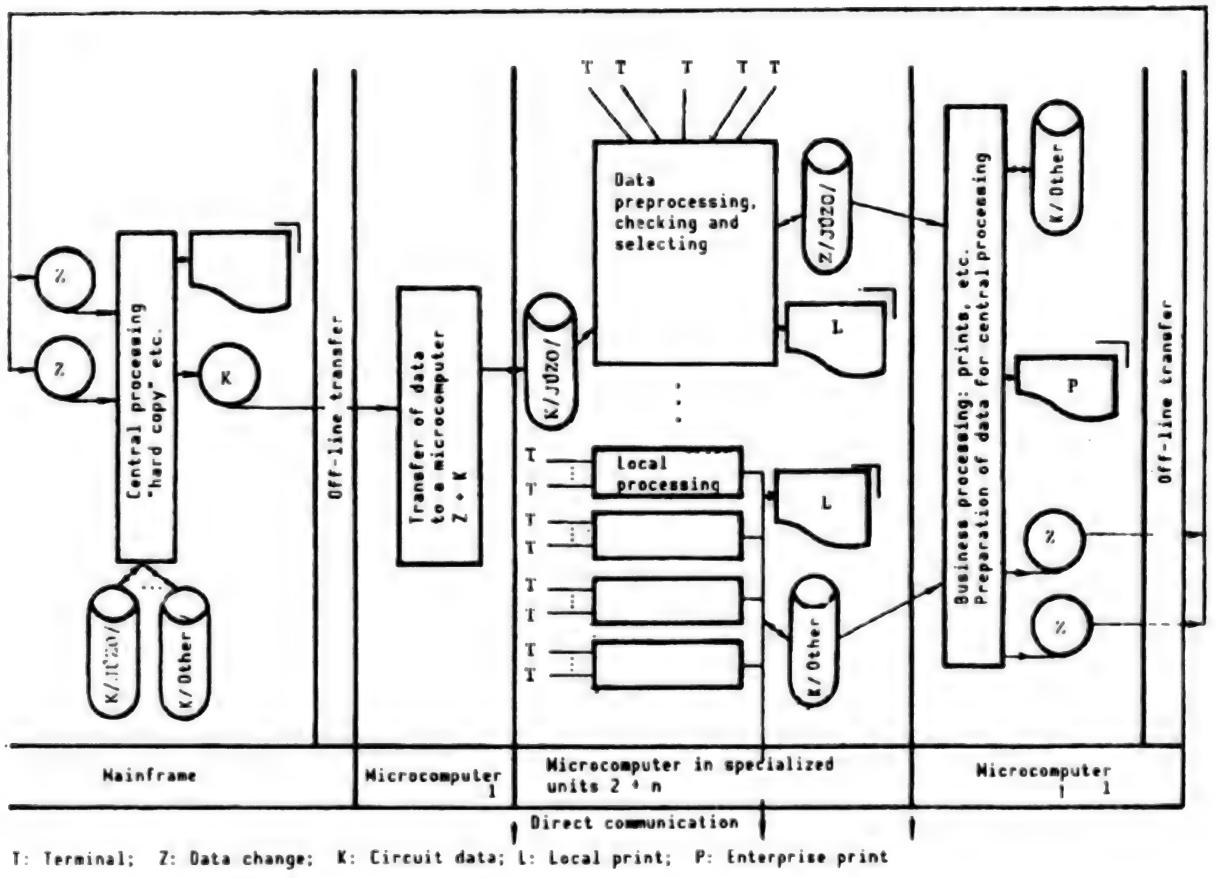

Figure 1.

our conditions, this area of computer use has one main problem: the absolute lack of good quality portable printers. The desired circumstance will obtain only when computers and printers will be as accessible as typewriters. A specific problem in the CSSR is the incomprehensive continued demand for information on preprinted forms—in correspondence as well as other areas. If we could dispose of this anachronism, the automated processing of texts would receive a great impetus. It would then be much easier to search for additional possibilities in the automated processing of texts, today represented abroad by desk-top publishing.

2. The local database and command/control tasks are unusually extensivemeans of utilizing micro- and personal computers in present-day practice. An even more extensive use runs into the following problems: a) the users' demands and conceptions of the capacity of the microcomputers and the standard program equipment, the lack of expertise on the part of the designers and their practical inexperience where the user is concerned quite often lead to problems such as the computer not being able to handle the suggested database; b) the program availability is too varied to successfully introduce a local database. The use of software, starting from dBase I to dBaseIII/+/, Dataflex and other products has one disadvantage: the paradoxical quick development of small computers facilitates a quick change in the design but, with few exceptions, the products are not always compatible with all the computers and the user is tied to presently applied technology. Since most of these producers and products (inexpensive for us) are short-lived, a real problem is created. It seems that only UNIX will ease the situation. c) finally, the design of the present "quasi-relative" databases formicro- and personal computers (the index sequential system organization)is not without problems. The scope of indices is growing very quickly and it is disproportionately overloading the capacity of disk memories.

In the CSSR, the most frequently used hard disks, 20M byte-45M bytedisks, are surprisingly small.

3. The spreadsheet processors are relatively problem-free. First of all, they are probably the most rapidly standardized processors (availability of various programs) and their scope of application is narrower than local databases. The most common problems with micro- orpersonal computers is the so-called "overfilled memory." This results in a concrete problem of the spreadsheet not being usable when there is more than one user per micro/personal computer. In other words, under the present conditions, this product will be applicable only in case of individual personal computers.

4. Applications programming probably represents the most troublesome area of all in the use of these types of computers. Because we will come back to this point later, we will bring up only the most critical issue. Much too often, it happens that computer specialists working on automation are using personal computers to carry out tasks in amainframe mode (manual coding), since that is what they are familiar with. Among other reasons, there is also the fact that parameters of general programming languages often surpass the capabilities of the same languages in many mainframes. If we consider other amenities, such as test routines and interactive programming, we can understand the reasons which lead to similar decisions. This is in part due to the outmoded notions on the part of micro/personal computer programmers who maintainat any price the principles of maximum saving of machine time at the expense of the advantages of automation. It is like desiring to travel by horse and buggy only because it is cheaper (without pollution, atthat) and it does not require periodic visits to the auto shop. It is worth noting that this is also the case when discussing the advantages of general program languages over assembler type languages.Holding onto this position creates many problems. However, the main ones are the unacceptable length of time it takes to accomplish thetasks, and the overtaxing of capacities. In practice, this often means an attempt to accomplish tasks using personal computers which would be too difficult even for a mainframe. Thus, we cannot ignore the principles of data processing and further discredit automation.

Claim V: "The gradual expansion of the use of micro- and personalcomputers and distributed data processing will lead to a situation wherethe users will be able to accomplish the majority of the local taskswithout the assistance of analysts and programmers...".This statement which could be paraphrased as "Each user is his own designer," has already caused much harm among the users of micro/personal computers. As we know from practice, this is not unreservedly true. Judging by the ever increasing demands placed on computer specialists who would like to promulgate the use of personal computers in many enterprises and institutions, it is not true at all. Above all, it is necessary to state that this notion regarding the accomplishments of automation tasks without programming is only partially valid and it will remain so in the future. Currently available programs for these computers, used in distributed dataprocessing, are not yet at the level of the so-called fourth generation programming. It seems that the best results are achieved when thezcomputers are used by specialists, i.e., analysts/programmers.

One of the main hurdles standing in the way of claim V becoming areality is the ever-present problem with the compatibility of micro- andpersonal computer programs. This is because operating systems are so varied (CDOS, MS-DOS, CP-M, and others). The fact remains that we cannot expect that the users themselves will maintain the automation approaches even in the case of transfer from one computer to the next. While changes in the hardware were exceptional in mainframes, in thecase of micro- and personal computers, we must count on changes as a certainty. This is dictated by the extensive and varied, ever changing technology on the world market. These problems with using micro- and personal computers for distributed data processing should disappear only after the implementation of the UNIX operating system mentioned above. It is well- known that UNIX is understood more and more as being the universal operating system. It is gradually being introduced as standard equipment for mainframes as well as for small computers of all brands.

The practical results obtained within the framework of the so-called X/OPEN Group, which is the driving force behind this operating system, are promising. On micro- and personal computers, UNIX covers all important programs singled out in point 4 above. In addition, no adjustment is needed when computers are changed. So far, the main problem with UNIX, when used in computers manufactured by foreign manufacturers and used in the CSSR is that this operating system is usually offered in 32-bit processors and these fall under the strict limitations regarding importation to socialist countries.

Limitations of distributed data processing on micro- and personal computers

If we are to specify the limits of distributed data processing on micro-and personal computers, all we need is to correct the initial claim, points 1-5. In the following commentary we touch upon how to proceed without exceeding the limits of these computers, but instead moving them. The following abstract is at once a summary and a conclusion of this article:

1. The distributed data processing (using micro- and personalcomputers) can be introduced at several levels. Experience shows that a procedure is particularly effective when these computers are introduced at two different levels: a) to introduce personal computers at work centers that handle a great number of local (limited by place) tasks by automating these tasks, we obtain valuable experience, take a load off the employees of corresponding units and create preconditions for the next step in the distribution of automated processing. The transfer of data is done mainly off-line, even in relation to the mainframe (central);b) we equip work centers with office-type microprocessors or interconnect personal computers only when we are able to fully meet the technological demands. This means that we cannot allow a situation wherein the automated flow of data in a network is interrupted by manual processing or where some users are discriminated against. This would result in automation having a negative rather than a positive effect.

2. To create networks of microcomputers, it is necessary to thoroughly analyze and prepare the organizational structures. The best way to achieve this is to simplify

these structures already included in the present reconstruction of our economic system. In cases where we arenot able to ensure relative stability of the organization, it is better to stay at the first of the above given levels of distributed dataprocessing or to consider introducing a terminal network. In any case,we must maintain a level of realistic optimism where the direct transfer of data in a communication network is concerned.

3. The connection of micro- or personal computers to a mainframe will,in the future, be a question of how extensively off-line data transfer will be used. The procedure shown in Figure 1 can be taken as one of the solutions. This is one area which can be considered a present and probably a future limitation of distributed data processing.

4. Micro- and personal computer technology can be used only for the purpose for which it has been designed. Because it is not the technology of a mainframe (even though, in today's computer world, the differences are diminishing) we have to first accomplish those tasks which require minimal or no programming. This is the only way we can achieve a situation where automation will be responsive to the reaction of ever changing demands and needs of the users. To broaden the use ofautomated text processing, it is necessary to abolish the outdated regulations on the use of preprinted forms, even if this should require legal and legalization adjustments. The core consideration regarding the use of micro- and personal computers is still the work with local databases. Increasing the capabilities of these computers can be done by focusing on those programs which, in today's world, are a part of the UNIX operating system. In all cases, however, the introduction of a local database must be preceded by a thorough analysis focused, among other things, on the clarification of its expected size. Just as years ago we gave priority to the use of general languages over the assembler type languages, we must now give priority to the use of standard programming as opposed to applications programming. There is no other way to shorten the time it takes to accomplish tasks and to make automation approaches more flexible in light of media changes. Considering that these computers are a part of this media the demand is ever more pressing.

5. As far as the extent to which the user units or rather their workers will be able to participate in the designing of automation approaches is concerned, there are limitations which as yet cannot be overcome. Therefore, a practical procedure is recommended. Each work center equipped with micro- and personal computers will have one or two specialists or designers. Assuming that they will not be overloaded with the old design system, their approaches should be quick, easily reparable, well documented and should represent the ideas of the users. As we see it, these are all spinoffs from the automation approaches which we would like to see last far longer than 20 years.

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Hungarian Computer Applications Firm Exhibits New Products

25020253b Budapest COMPUTERWORLD/ SZAMITASTECHNIKA in Hungarian 3 Jun 89 pp 1, 3

[Article by Huba Bruckner: "Szamalk: Well Thought-Out Integration"]

[Excerpts] It may have been intended as rhetorical but it may have been out of modesty that Miklos Havass, director general of Szamalk [Computer Applications Enterprise], began his briefing at the fair by saying that we should not expect earth shaking novelties at pavilion 43 of this year's BNV [Budapest International Fair], where his firm was exhibiting. [passage omitted]

It turned out that they had brought to the fair products and user systems which had proven themselves and not rarely had passed the test on the world market.

We could see the MAS-MCS production control system. Even the largest Hungarian enterprises can base their computerization ideas on this with confidence as the program package is intended for a multiprocessor, mainframe environment. Development of user systems is under way at Videoton and the BHG [Beloiannisz Communications Engineering Factory] and an additional six firms are interested in the program packages.

It is characteristic of the capacity of the MAS-MCS that at Videoton, after the system is completely built up, 150 personal computers will be connected as terminals to a network combining the power of the mainframe computers.

In regard to applications possibilities we can already find throughout the country the MTS configurations, which can be regarded as the little brothers of the MAS-MCS, in which XT and AT computers work together in a Novell network. They have already installed a version based on the Mikrosztar 32 in 120 places.

In regard to the applications areas for computerized design Szamalk is placing ever greater emphasis on architecture. The interesting feature of the Raster Plus graphic CAD system is that it can work with data files which can be connected to it. So there is no obstacle to integrating into the designing system the budgetary, labor or material norms of the country which is using it.

They have already sold more than 30 of the Genesys expert systems, version 2.0. The circle of applications was recently expanded from turbine design to insurance counselling. Domestic and foreign interest in knowledge bases loaded for a concrete purpose is growing, in addition to the interest in expert system shells.

We could hear that there is a trend which has lasted for several years but which is now strengthening—using redesigned Makrosztar configurations expanded with processors of Western origin, in the place of mainframe computers of socialist manufacture.

It is a real sensation that talks with the DEC firm, the second largest manufacturer of computers in the world, regarding sale in Hungary of their products, are well advanced. The visits of high ranking DEC leaders in recent months also indicate that DEC again wants to get onto the Hungarian market. At the BNV Szamalk exhibited the DEC VT 320 and VT 340 displays. The price of the former is 67,000 forints; the latter, a device with 260 x 480 pixel resolution, will cost 280,000 forints. Anybody who brings the money can take one away.

Naturally the assortment will expand in the future and as a system integrator Szamalk will also count on the products of DEC, just as it is expanding its offering with laptop computers.

The modern VAX-A-FAX telefax device, which has been sold since the Orgtechnik-Compfair last year, could be seen this time in a Mercedes automobile, proving its high degree of mobility. It can be connected via a radio transmitter to the landline transmission network. It was a surprise that Szamalk has signed an agreement with the mammoth software firm Computer Associates. The product scale of CA is the largest in the world in its area; it offers products for everything from personal computers to mainframes and networks.

Although much was said about personal computer networks and mainframes we could not learn which of the two the structure of Szamalk will most resemble in the future. Will it remain a giant enterprise, or will it be transformed into some sort of grouping of smaller economic units?

Hungarian Software To Facilitate Robot Programming

25020265b Budapest COMPUTERWORLD/ SZAMITASTECHNIKA in Hungarian 22 Jul 89 p 2

[Article by Attila Kovacs: "Robot Pantomime"]

[Text] Although we are still in baby shoes in the use of robots a number of domestic institutions are trying to obtain usable results in developing devices connected with them. One of these institutions is MTA SZTAKI [Computer Technology and Automation Research Institute of the Hungarian Academy of Sciences]. Its graphic motion programming software Mosy (MOtion SYnthesizer) replaces with motion simulation programming, which can be done off-line, that is on a computer not connected to the robot, the frequently time-consuming, expensive on-line training which demands great dexterity.

"On the one hand, off-line robot programming makes economic savings possible as it does not take the time of the robot to train it for the next series of operations," said Miklos Bathor, developer of Mosy. "On the other hand, the robot program can be tested under simulation conditions; for example, the correctness of it can be checked with the aid of conflict studies." It is a fact that the motion simulator program, which can be run on IBM-compatible PCs, reduces the downtime for robots. This means that the robot can participate in training while the programming for new tasks is under way.

At present Mosy can be used immediately, without adaptation, for two types of robots—the six degrees of freedom Puma and the four degrees of freedom Scane. In each case the user himself can provide the parameters for the length of robot arms. The robot program can be used in prepartion for small and medium series manufacture, especially in assembly technology, and in areas of computer aided design and manufacture (CAD/CAM) where the path to be followed by the robot is given in rectangular coordinates.

The reference sites for Mosy are the Machine Manufacturing Technology Faculty of the Budapest Technical University, where it is used in instruction, and the Jaszberenyi Chipping Machine Factory, where it is used in simulation of an IGM robot.

Another SZTAKI achievement is the Modbuild (Model Builder) program package with which one can define bodies delimited by plane, cylindrical, conical and spherical surfaces, building up either a nodal surface hierarchy or using transformation and combination of existing bodies. Both programs can be found in a number of engineering developmental insititutes. Typical applications, in addition to instruction and robot programming, are design and display of fastening devices, animation and simulation of manufacturing cells. They are used in every area where the goal is display of a series of moving pictures of objects which move according to a program.

FACTORY AUTOMATION, ROBOTICS

GDR's PolyCAD Package Described

23020067 East Berlin NEUE TECHNIK IM BUERO in German May-Jun 1989 pp 86-88

[Article by Dieter Herden, Rolf Ludicke, Werner Tischer, and Claus Wippich, CAD-CAM Center in the Kombinat Polygraph, Leipzig: "PolyCAD—a Modular and Data Bank-Supported CAD-Package for Industrial Use Under DCP"]

[Text] 1. Introduction

Great flexibility and short development to production and processing times require the design and deployment of thoroughly rationalized solutions from design to fabrication. At the core of these rationalized solutions are CAD/CAM applications whose design and introduction require software which can be integrated and adapted to prevailing task requirements.

Internationally, talk is about the application of a new CAD-technology characterized by the use of a second generation of CAD-systems.

In contrast to the graphics systems often used especially in machine production, these CAD-systems are characterized by providing an increasingly thorough, computation-supported treatment of the partial processes from design to the fabrication of parts and assemblies based on an implemented data model.

The data model or the product data model secures for the user various views of the work object (individual part, assembly, etc.), for example:

—a design view through a description of the functional elements,

—a construction view through a description of the geometric elements,

—a technological view through a description of the processing elements.

Additional views of, for example, technological expenditures and costs, based on the data model are quite possible. Thereby a large part of the specific problem set will not be put into source codes but will be expressed in the structure and content of the data model. Consequently, the essential advantage of this conception is that the necessary flexibility in the CAD-system can be realized through modified or new operations on the data base. Included from this point of view are, for example, drawing or other graphic representations, the parts list, the coordinate list, as a prerequisite for the numerically guided manipulation, among others, the various views of this data base.

The calculations, simulations, selection processes and variant comparisons carried out on this data base can lead to an expansion of the data base in the form of result data elements.

Nevertheless, at present there is a problem because general statements for effective description or notation in terms of the data, for example, the elements of function and form, are still being worked on or are being refined.

2. Second Generation CAD-Software

The second generation of CAD-software is internationally characterized in terms of the following criteria:

—functional and structural modularity for adaptation to specific set of problems,

—integration capability of the CAD-software through defined splice points, separating program and data segments, which are particularly well suited for data transfer to international standards, such as the GKS-standard, the IGES-format, among others,

—provision of graphic and alphanumeric procedures performed on a product data model which requires the integration of data bank functions into the CAD-system for the management of the product data model, and of modules for the realization of graphic and alphanumeric tasks performed on this data model,

—providing a system and project management for process supervision by the user working with this system, that is, the management of access rights to programs and data, registration and supervision of the working conditions, configurational capability of the system with respect to entry and exit data, their structure and combination including the data formats,

—insuring the networking capability of the software,

—supporting the adaptability of the software to special problem situations through software tools as implements of software development.

If one analyzes in this respect the CAD-software packets currently in development or use, the extent and involved nature of the task to be solved becomes clear.

The general goal for the further development of CAD/CAM-systems in the fields of mechanics, construction and projection should consist of reducing as much as possible the large number of currently used software packets and to bring about an orientation toward a few, very efficient CAD/CAM systems where both the 16- and 32-bit computing techniques may be applied. At the same time, a thorough clarification of the source, in a higher programming language, is a requirement for adaptations and also for the development of a thorough computational support in the sense of the stepwise realization of CIM-solutions.

3. PolyCAD System Development

After an analysis of the CAD packets for 16- and 32-bit computing techniques either available in the GDR or to become available in the near future, the CAD/CAM Center in Kombinat Polygraph Leipzig was faced with the task to develop a portable software system which, based on a product data model, provides for a thorough computational support, from planning to the NC-guided fabrication of a part or an assembly and, furthermore, offers additional possibilities for task integration.

This CAD-system should also exhibit sites for intersection with other CAD-systems used in the GDR (exchange of drawing files) and, simultaneously, sites for intersection with data bank systems in use (for example, REDABAS-2/3) and with user-defined data elements in order to permit a coupling with these systems. It became clear during the conceptual phase that the problems which emerged from the areas of construction, projection and technology often bordered on typical ready-made softwares for graphics production systems and data bank work.

One problem arose from the fact that the available software for graphics production for 16-bit microcomputers was, in general, unable to produce and manage extensive collections of data over and above the production of itemized lists and other support data. In particular, only the makings for the generation of itemized lists were available.

Calculations, variable comparisons, selection processes according to standard parts and standardized assemblies (stores, etc.) were generally not possible in connection with drawing production.

The compressed data content of the drawing and unit list files of the previously used systems was insufficient for a number of added on problems.

Because of this, the CAD-packet PolyCAD was developed on the basis of a freely editable product data model which, on this basis, makes it possible, on the one hand, to produce high level drawings, comparable with internationally known systems, but, at the same time, provides the possibility to acquire a number of data, needed in the construction process, during the production of the drawing or through a preceding or following added subroutine, and to use them in specific modules.

The programming of the software modules, briefly characterized in the following, was done in T-PASCAL (V5).

3.1. System Components

PolyCAD was strongly modularized and must be listed in the category of data bank-supported CAD-packets.

Figure 1 shows the schematic buildup of the CAd-packet PolyCAD. Thereby it becomes clear that on the basis of a data base which is freely editable by the user, the partial functions of drawing production, data bank work and modular work (calculations, production of unit lists or evaluations) can be called upon at an operational control level.

3.1.1. Drawing Production System (PolyCON)

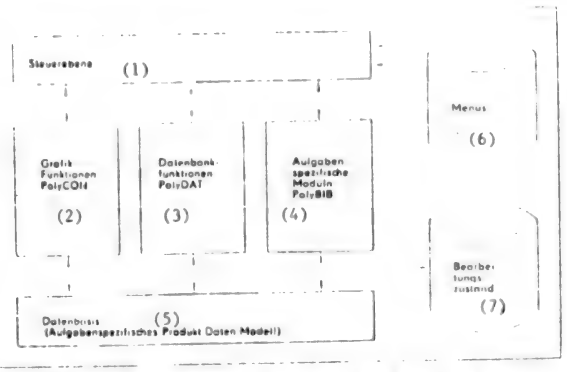

Figure 1. Schematic Buildup of PolyCAD

Key: 1. Operational control level—2. Graphic functions PolyCON—3. Data bank functions PolyDAT—4. Task specific modules PolyBIB—5. Data base (task specific product-data-model)—6. Menus—7. Work status

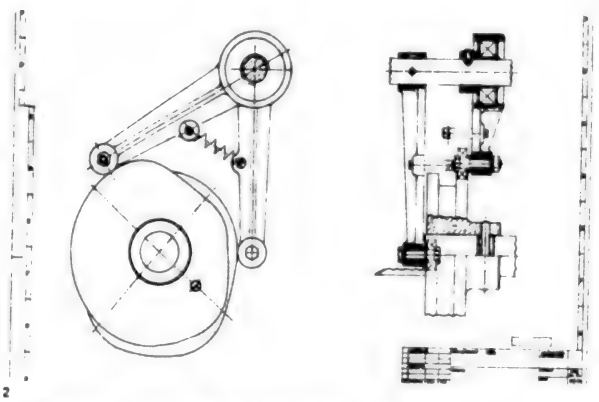

Figure 2. Drawing produced with PolyCAD (sector)

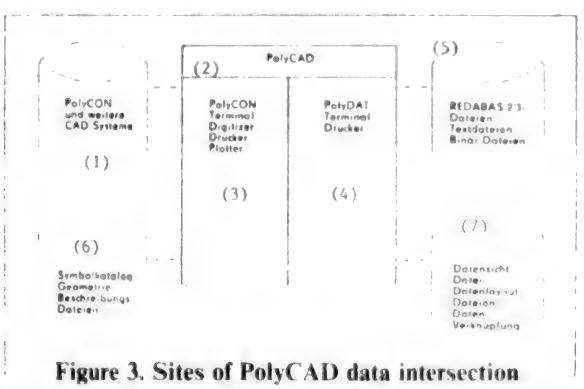

Figure 3. Sites of PolyCAD data intersection

Key: 1. PolyCON and additional CAD-systems—2. PolyCAD—3. PolyCON terminal digitizer, printer, plotter—4. PolyDAT terminal printer—5. REDABAS-2/3-data, text data, binary data—6. Symbols catalog, geometric descriptive data—7. Data view data, data layout data, combination of data

The PolyCON module is a 2-D-construction packet with the typical functions for manipulation of the basic graphic elements and symbols. It encompasses sector and plane section work (1024 picture planes) and extensive output possibilities to monitor, printer, plotter and, in the future, also to the laser printer RX 4045 and laser illuminator CLS 2090.

The drawing production module should respond to the following demands:

—management of access rights to programs and data by presentation of password and user name, automatic supervision and recording of access and changes,

—production of the script field, supported by the data bank and in accordance with standards, and management within a script field data set; script field information is blended into the drawing only for publication purposes,

—the production of drawings is achieved through a menu-guided, free management of dots, lines, circles, arcs, text and pre-prepared elements (symbols, partial pictures, data describing geometry). A rational command language for these actions is available to advanced users,

—script field information is contained in extra data sets and is blended into the drawing only for publication,

—coordinate lists of individual picture elements and additional data extracted from the picture, or data which are to be registered in parallel with the process of picture production, must be made available as user-defined data sets,

—new or given graphics must be produced or recalled from coordinate lists,

—symbol catalogs must be capable of being related to basic data sets,

—the possibility must be given for the transfer of basic data into selected result data sets (analogous to projection operations) when working with symbols,

—insuring script field generation from alpha-numeric data produced through dialogue and/or from the object description of the data bank,

—the system must be capable of co-managing working conditions, the entry of corrections with date and operator, and user groups,

—menu texts must be easy to change,

—the further development of the program system must be assured by the availability of source programs.

The construction module is started by introducing the user's name in the corresponding drawing catalog.

The drawing numbers assigned to a given user name in the drawing catalog are prepared through a preliminary central instruction and have a binding character for the entire work process. After the selection of a drawing number, one has the following components of the product data model accessible for work:

—the drawing,

—the script field and

—additional data sets, for example the list of coordinates.

From the script field data set, parts list information is obtained as work proceeds. Further on, the coordinate list serves as starting material for NC-programming. Similarly, new, rough drawings can be generated with a coordinate list, or existing ones called up with reference to the form element coordinates contained in the drawings. This data set which accompanies every drawing can be produced and processed with the full efficiency of the data bank. The structure of such data sets is to be determined before their initial creation. Thereby an adaptation to changing user demands can be achieved at relatively small expense. In order to achieve extensive independence of the graphic packet from the hardware and the implementing basic graphic software (graphic executive), all graphic operations take place in the 2-D-model plane under which, in a physical plane, the user coordinates will be transformed into the device coordinates of the basic graphic software (in the present case, DCP/GX) with its special device drivers.

In this manner, an exchange of the basic graphic software, for example, for an implemented GKS system or BGI (Borlands Graphics Interface) becomes possible and, on the other hand, the expansion in the model plane is permitted toward a 3-D/2-D-transformation.

Figure 2. shows a drawing produced with PolyCAD.

3.1.2. Projection Module

The emphasis in the use of this module consists of a data bank-supported work-up of a project with the possibility of using graphic functions.

The program is divided into an efficient data bank system for the alphanumeric and graphic information about the object to be projected (building groups, machines, plant components, among others), and the implemented projection logic. Entry at the operational control level occurs with the user's name in order to clear the access rights to programs and data sets. In the projection logic, typical data bank functions are coupled with problem-specific computational and selection algorithms. The projection result can be graphically presented in the form of a survey layout and can be further processed through a task-related dialog.

Graphic actions (labelling of a graphic object or symbol for identification, obliteration or copying) will be first registered in the data model and then become graphically visible on the screen. The integration of a data bank

system with all typical functions in the PolyCAD program system guarantees a coupling with other systems through data transfer. For understandable reasons, no particular data bank format will be defined but this definition will be left to the user because the user is often tied to given data sets. In addition to widely used data bank formats, such as REDABAS-2 and -3, user-defined formats can also be worked with.

The user-oriented formation of the operational control level is characteristic (see Figure 1); it disposes over loadable menus, and oversees and registers the work status, at any given time, in the projection or construction process.

The typical performance characteristics of the data bank are:

—maximal 4,096 byte long data strings of maximally 256 elements,

—Baier-Baum-index processing.

The following data types can be processed:

string, char, Boolean, shortinteger, integer, longinteger, byte, word, real, single, double, extended, complex, datum, logic, symbol chain, numeric, text data, graphic and data sets. The last three data types are PolyCAD-specific and represent pointers to such data sets. They are realized as strings. In the system, there are possibilities for defining rules for linking source and target data complements, and for storing this definition in data sets.

Thereby an opportunity is offered for linkage with knowledge-based systems.

4. Application of the PolyCAD Program System

The PolyCAD program system was developed for the fields of machine construction, electrotechnology and similarly situated industrial domains.

The currently available working versions are being tested in various Kombinates and the results of industrial testing taken into consideration in the course of development. An important case of application is present in polygraphic machine construction itself where, in the Druckmaschinenwerk Leipzig, a pilot project is being prepared for a thorough solution, from the production of drawings to NC-programming, by means of PolyCAD. An additional emphasis is provided in Kombinat Polygraph, consisting of the coupling of PolyCAD with PROCAD.

5. Hardware-Technological Requirements

At this time, PolyCAD can be run on the 16-bit microcomputers A 7150G, EC 1834 with graphics adapter under DCP, and on IBM-compatible microcomputers under MS-DOS 3.2. The complementing peripherials stress the assortment which is currently distributed by Robotron. A graphic version will be prepared for the RX 4045 laser printer by Xerox and the CLS 2090 laser illuminator by Siemens for producing ready-to-print technical documentation (drawings, basic projection materials, standardized partial views, among others).

6. Distribution and Servicing

The PolyCON 2-D-construction packet in version 1.0 is manufactured in TGL-compatible dimensions.

In the second half of 1989, version 2.0 will follow with the following modules:

—Drawing management and research as well as

—Data bank supported symbol or standard part work.

Distribution of the A 7150G is through:

VEB Robotron-Electronik Dresden Department KSRS P.O. Box 240 Karl-Marx-City, 9010.

EC 1834 is distributed through:

VEB Robotron-Buromaschinenwerk "Ernst Thalman" Sommerda Software Center Weissenseer Street 52 Sommerda, 5230.

The PolyDAT program module (non-standard data bank system) can, at present, be used in industrial testing and is being tested in the design of projection systems with varied task constellations.

Further information with respect to the possible use of this software with other computers is provided through the Polygraph CAD/CAM Center:

VEB Polygraph Druckmaschinenwerke Leipzig CAD/Cam-Center Wachsmuth Street 4 Leipzig, 7031. (NTB 3822)

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INDUSTRIAL AUTOMATION

Hungarian Development of Composite Insulators Discussed

25020264 Budapest ELEKTROTECHNIKA in Hungarian No 6, 1989 pp 203-206

[Article by Alajos Bognar, Pal Szaplonczay, Marton Teglas, Sandor Csecsody and Dr Endre Zelenyanszki, of the Electric Industry Research Institute: "Development of Composite Insulators for High Voltage Switching Equipment"]

[Excerpts] The further development possibilities for traditional porcelain insulators are being essentially exhausted. Some characteristics of these insulators are less and less suitable for the new modern requirements (the need for increased reliability in addition to increased demands) which appear for both overhead line and high voltage substation insulators.

In connection with high voltage, hollow body insulators, the reliability problems of traditional insulators have become more acute, especially in equipment constantly subject to internal pressure (e.g., the SF_6 insulated equipment). In the present, very compact substations the explosion of a device (whether due to internal failure of the device or a fault in the insulator) causes secondary damage greatly exceeding the price of the device. The further development of device design and the appearance of new principles (e.g., electronic and optically connected meter switches) poses new requirements for insulators.

All of these factors contributed to the fact that the technical and economic conditions for the industrial introduction of hollow body composite insulators, the most promising family of synthetic insulators suitable for outdoor use, ripened in the second half of the 1980's.

In the insulation technology main department of the VKI [Electric Industry Research Institute] we have been dealing intensively with the development of outdoor high voltage insulators since 1972 (between 1972 and 1979 in cooperation with the VEIKI-MUKI [Electric Power Industry Research Institute] and simultaneously with the development of a modern manufacturing technology for them. As a result of the latter we developed procedures, protected by patents, offering rational solutions for series manufacture and for the individual manufacture of special insulators and these aroused the interest of leading world firms dealing with heavy current. The project described in detail below was first realized in the form of a manufacturing line at the Swiss BBC firm (it is now called ASEA-Brown Boveri, ABB for short). The latter works on the basis of a VKI technological license using equipment designed by us, in part delivered by us, which was put into operation successfully.

1. Design of Composite Insulators

The essence of the design of composite insulators is that an epoxy core (rod or pipe) reinforced with glass fiber provides the mechanical strength (tension in the case of rod insulators and flexure or internal pressure in the case of hollow body insulators) while the necessary external electrical strength is ensured by a screen system made of flexible plastic. Metal fittings at the ends serve to connect the insulators to the load. [passage omitted]

3. The Visil-Composite System

By the above registered trademark we designate the technology developed at the VKI and the manufacturing line to realize it; it is used to produce composite insulators with a silicone rubber screen system.

The two-component liquid silicone rubber (LSR) goes into the VISIL-MIX mixing-feeding equipment together with a coloring paste. The material, compounded in the proper ratio, goes into a mobile pressure tank which, in addition to receiving the compound, serves to transport it to the casting machine; when the tank is under pressure the compound flows from the tank into the casting forms.

We developed essentially two methods for the casting procedure as described below.

a. The Metal-Rubber (M-G) system, in which we use a metal casting form consisting of two halves. This is attached to a hydraulically operated casting machine (a tool locking unit). The metal tool is electrically heated and this is freely programmable by the control unit. This almost completely automated procedure is very productive and makes possible the production of insulator units 0.8 to 2 meters in length in one casting step. The procedure is especially advantageous in mass production where the mechanization and automation supplemented by good work organization yield short technological times and small live labor costs. The disadvantage of the system is the relatively large investment cost, which is amortized when manufacturing a large number of units.

b. The Rubber-Rubber (G-G) system, which uses rubber casting forms to produce silicone rubber screens. The tool consists of heatable rubber rings corresponding to the form of the screens which are held together by fastening elements. The assembled tool set is placed in a vacuum chamber and then flooded from below with liquid silicone rubber. This procedure is used primarily to produce small numbers of units, when developing prototypes or preparing items for marketing purposes. The investment cost is substantially less than that for the M-G system. At the same time, its productivity is less and the live labor demand is greater.

We put the above described Visil-Composite System manufacturing line into operation, with a two-machine M-G system, at the Baden factory of the Swiss ABB. [passage omitted] We also built a fiber optics system into the glass fiber reinforced tube; with this it is possible to

derive the ground potential information which becomes a light signal at high voltage.

Construction of additional Western European systems is now under way and we are studying the possibilities for domestic use together with the Ganz Electric Works.

LASERS, SENSORS, OPTICS

Sweden: New Protective Welding Helmet Developed

23020077p East Berlin TECHNISCHE GEMEINSCHAFT in GermanNo 6 1989 p 3

[Text] Sweden's Hoernell Electrooptics AB has developed a heat-dissipating welding helmet with eye-protecting glass filters that darken automatically as soon as the welding process commences and permits the passage of normal light once the welding process is over. The new [glass] product was introduced as "speed glass".

The [helmet's] replaceable glass filters are one-piece laminates consisting of liquid glass crystals, polarization filters and a filtering layer which reflects ultraviolet and infrared light. Three photocells regulate light transmission through the filter, up to 100 times in 10 milliseconds. The photocells are controlled by a battery-operated electronic device.

The welding helmet weighs 450 grams. The welding process is thus [made] more efficient since the welder has both hands free and need not make any adjustments to his protective eyeglasses.

MICROELECTRONICS

GDR: Improved Manufacture of Ceramic Housings for Microelectronics

23020085p East Berlin FEINGERAETETECHNIK in GermanJuly 1989 p 307

[Text]The Ceramics Works Combine in Hermsdorf has developed and put into production a process for galvanic nickel plating of ceramic housings for memory and processor circuits—a novelty for the GDR. Heretofore, semifinished goods had to undergo nearly 20 processing steps involving manual treatment. Automatic devices, program-controlled by microcomputers, are now taking over the processing tasks and are eliminating substandard departures from the technology. After completion of the final phase [of preparation] in May [1989], at least a threefold increase in nickel plating productivity is expected.

In the fall of 1988, the Hermsdorf plant began mass production of multilayer ceramic housings, a new development on the international scene. The Microelectronics Combine in Erfurt is using this product for housing circuits. The oxide ceramic products used are particularly suitable and, by virtue of their high sealing density, insure the chips' immunitiy to atmospheric moisture. According to experts, this multilayer process, developed in the GDR, is almost doubly as productive as comparable technologies applied up to this point in time.

Printed Circuit Designing System Wins Budapest Fair Prize

25020253a Budapest COMPUTERWORLD/ SZAMITASTECHNIKA in Hungarian 3 Jun 89 p 1

[Article by Huba Bruckner: "A Prize Winning Product"]

[Text] The EMG 19100 printed circuit designing system of the Electronic Measuring Instruments Factory [EMG] received the fair's prize. The goal in developing the configuration, built for a DEC PDP-11/73 compatible computer and a high resolution intelligent display, was to realize an integrated system which would help the work of engineers by producing the information needed for manufacture of printed circuit cards, from the design of the circuit diagram to checking of the assembled cards.

The multipurpose equipment could have won a fair certificate last year too as those interested could have seen it at the 1988 BNV [Budapest International Fair] as well, and it could do as much then as it can today. Of course it is no problem if the certificate should recognize the market success of modern products but unfortunately this is not the case here. For the time being the EMG 19100 is in operation only at the developing firm in our country and at a Soviet electronics enterprise.

But the EMG 38100 multichannel analyzer really is a new item. The nuclear instrument, primarily to record and process gamma spectrums but it can also be used in the area of X ray and neutron spectrography, can be connected to IBM PC/XT and AT computers. It has the advantage that a rich assortment of personal computer software prepared for signal processing can be used as well. Thanks to the large internal storage capacity of the EMG38100 and thanks to the data compacting procedure used it can also work in an autonomous mode for data collection purposes. This instrument is unique on the socialist market. By next year, perhaps, we will be able to report market successes and not only a prize at the fair.

GDR: Wafer Stepper Enters Serial Production at Carl Zeiss Combine

23020078p East Berlin NEUES DEUTSCHLAND in German12 Jun 89 p 2

[Text]At the Carl Zeiss Combine in Jena, in the shop for the construction of precision optical instruments, the serial production of AUR2 automatic wafer steppers has begun. In the microelectronics industry the devices are necessary for setting up the production of monolithic memory circuits at the 1 Mbit level of integration. The AUR2 can also carry out preliminary processing for 4 Mbit technology. Wafer steppers figure as one of the

devices crucial to the microlithographic manufacturing process that includes 450 technological steps on nearly 70 different devices.

The AUR2 optically transfers the complicated component structures of the circuit to be produced, from masks to silicon wafers. At the same time, the structures undergo an 80

reduction in size. In the automatic mode of operation, this procedure is repeated around twenty times per wafer. For example, for a 16 x 16 image field, structures with a conductor "width" of scarcely a micron can be produced. The level-to-level stepping precision is given by experts as plus or minus 1 micron.

NUCLEAR ENGINEERING

Three Year Operation of Hungarian Cyclotron Reviewed

25020259 Budapest FIZIKAI SZEMLE in Hungarian No 5, 1989 pp 194-196

[Article by T. F.: "Hungary's Cyclotron is Three Years Old"]

[Text] On 14 December 1988 the physics work committee of the Debrecen Committee of the Academy and the nuclear physics and applications group of the Lorand Eotvos Physics Society held a full day scientific session at ATOMKI [the Nuclear Research Institute] with the title "Hungary's Cyclotron is Three Years Old." The purpose of the session was a review of the more important results achieved by the cyclotron in the areas of atomic and nuclear physics basic research and in practical applications. The program was participated in by about one hundred people from Academy research institutes, various universities of the country, enterprises combined in the Debrecen Scientific Technical Park, clinics, the National Atomic Energy Committee, etc.

The Hungarian cyclotron was put into operation at the Nuclear Research Institute of the MTA [Hungarian Academy of Sciences] in Debrecen in November 1985. The cyclotron can accelerate hydrogen and helium nuclei to a maximum energy of 20-26 MeV, with significant (25-50 microamperes) intensity. The accelerating equipment was designed and manufactured in the Yefremov Scientific Research Institute for Electrophysical Equipment in Leningrad; the bulk of the physical measurement equipment was developed domestically. Creation of the cyclotron laboratory was the largest scientific investment in Hungary in the first half of the 1980's. In addition to the accelerator, the measurement equipment and the beam channels serving to conduct the accelerated particles the laboratory includes a measurement and computer center, an isotope laboratory, an area for medical applications, laboratory facilities, workshops, etc.

Basic research, applications and developmental work programs are conducted with the cyclotron. Basic research includes nuclear spectroscopy, nuclear reaction and ion-atom collision studies. The applications areas are isotope production, material studies with nuclear physics methods and radiation with charged particles (or neutrons). The developments connected with the cyclotron involve accelerator physics and nuclear electronics.

Starting up the cyclotron transformed the life of ATOMKI; in the course of the investment the fixed assets of the institute doubled and it became possible to acquire very valuable, modern instruments. The everyday work of about fifty institutional colleagues is connected with the laboratory. The very valuable equipment of the laboratory is at the disposal of other institutions as well. The new research possibilities also aided the building up of new international contacts and ATOMKI is linked ever more broadly into international scientific work.

In the spring of 1986 the cyclotron achieved the parameters guaranteed in the specifications and it has operated regularly ever since. In the first three years about 4,100 hours were turned to basic research and 2,000 hours to applications; maintenance, repairs and accelerator development took place in the remainder of the time.

The atomic physics studies are directed at a study of the electron and electromagnetic (X-ray) radiation arising in ion-atom collisions. With a special electron spectrometer developed at ATOMKI they succeeded in achieving a better energy release than in earlier studies. Studies done with the special technique and posing new problems led to internationally new results and organically supplemented corresponding measurements done at Dubna.

Most of the user time in the first three years of operation of the cyclotron, about 2,100 hours, were turned to basic nuclear spectroscopy research. The purpose of the studies was a systematic examination of the structure of indium and antimony nuclei in a broad nuclear range with complex electron and gamma spectroscopy methods. The studies resulted in fundamentally new information about 11 indium and antimony isotopes. This includes observation of more than 670 gamma radiations (350 of them new internationally) and 230 nuclear levels (105 of them new internationally) and a determination of their characteristics; it includes a uniform quantum mechanical description of the nuclear structure with a new nuclear model, the recognition of new systematic interdependencies in the nuclear structure, a clarification of the role of different types of reactions between the protons and neutrons forming the nucleus, etc. The superconducting magnetic electron spectrometer developed by ATOMKI contributed greatly to the success of these studies; it is a unique piece of equipment for similar type cyclotrons on a world scale.

The chief tool for the nuclear reaction research being done with the cyclotron is the scatter chamber and

multidetector measurement system developed jointly with the Particle and Nuclear Physics Research Institute of the Central Physics Research Institute (KFKI). The research was directed at a clarification of the potential behavior of a nuclear physics model describing the scatter of charged particles. In the near future they plan to start measurements requiring particle identification.

On order and as part of outside cooperation they have done nuclear analytic studies to determine the oxygen content and the presence of other trace contaminants in high purity metals (e.g., aluminum and gallium). They have also studied the element composition of glasses and lubricating oils. They set up (with OMFB [National Technical Development Committee] support) a measurement laboratory for the domestic adoption of the surface activation technique which makes it possible to check wear processes (corrosion, erosion) in parts. Radiation for a similar program at the MTA Isotope Research Institute in Budapest was also done with the Debrecen cyclotron. Isotope production is an important applications area for the cyclotron. The largest user of the isotopes produced is medical diagnostics. At present they are producing Ga-67 and I-123 isotopes for medical purposes, in cooperation with the MTA Isotope Research Institute; these are used for diagnosis of tumorous and inflamed changes and for heart tests. Domestic production of the isotope In-111 is being introduced. There are also experiments to produce the short half-life isotopes C-11, O-15, N-13 and F-18 and use of them as compound markers. They produce a stripped Na-24 isotope for the Ecology Faculty of the KLTE [Lajos Kossuth Science University] which is used to study the water metabolism of trees.

In addition to the analytical tasks the neutron sources of the cyclotron are used for medical biology, plant stimulation and dosimetric radiation purposes. The chief goal of the radiation work done in cooperation with the Radiology Clinic and Medical Biology Cyclotron Laboratory of the Medical Sciences University in Debrecen is to get radiobiology experience for neutron therapy studies. Similar cooperation will begin in the near future with the National Radiobiology and Radiohealth Institute. Precise nuclear data are also important for solving the practical tasks; the variable energy Debrecen cyclotron provides good opportunities for measuring these data. In recent years they determined the excitation function connected with production of the Ga-67 isotope. Significant developmental work, making instruments and aligning activity were needed for the successful realization of the applications mentioned. These include development of the radiation beam channels, adaptation and alignment of gas target neutron sources, installing a neutron collimator which could also be used for human purposes, etc.

TELECOMMUNICATIONS R&D

Ferrite Devices Developed at Hungarian Telecommunications Institute

25020258b Budapest HIRADASTECHNIKA in Hungarian No 2, 1989, pp 56-62

[Article by Dr Peter Barsony, Pal Gyuri, and Mrs Daniel Sztaniszlav, Telecommunications Research Institute: "Modern Microwave Ferrite Devices"]

[Excerpts]

Summary

The theoretical and practical results achieved in the course of research and development on microstrip and strip line circulators and isolators made it possible to prepare modern microwave ferrite devices at the Telecommunications Research Institute. This article is a review of this activity. [passage omitted]

2. Ferrite Materials

[Passage omitted] The microwave ferrites developed at the TKI [Telecommunications Research Institute] made it possible to build the development of circulators and isolators on a domestic base.

The most important parameters of modern ferrite materials are summarized in Table 1.

Table 1. Characteristics of Modern Ferrite Materials

Material Type	4 Pi M_s in mT	Delta H in KA/m	tg delta in $x10^{-4}$	Thermal coefficient in alpha (+50 percent) degrees C^{-1}	Frequency range used in GHz
YFe garnets	58-180	4.0-8.0	lessthan10	-0.05to0.20	lessthan10
Very low loss garnets (Y-Zr)	100-137	1.0-2.3	lessthan 5	-0.30	4-8
Temperature Stable Garnets (GdCalnV)	27-60	5.6-9.6	lessthan10	-0.01to-0.09	lessthan 2
Li ferrites	210-370	35-40	lessthan10	-0.08to-0.10	10-18
NiZn ferrites	480	8.0	lessthan10	-0.25	greaterthan18

3. Design of Strip Line and Microstrip Circulators

[Passage omitted] It was possible to rework the results of Bosma developed for symmetrical strip line circulators (H. Bosma, Junction Circulators, Advances in Microwaves, Vol. 6, Academic Press, 1971) in order to design microstrip circulators and with the introduction of an experimentally determined constant multiplier we derived equations which could be used well in practice (P. Barsony, A Few Problems of Microstrip Circulators, TKI Yearbook, Technical Press, 1975-1977).

Determining the susceptance slope of the circulators is simplified by the recognition that we can calculate it by multiplying by a constant if we know the susceptance slope of the constituent resonators (F. J. Rosenbaum, Integrated Ferromagnetic Devices, Advances in Microwaves, Vol. 8, Academic Press, 1974). The constituent resonator for strip and microstrip circulators is a ferrite resonator connected with one line, so the studies can be limited to this. In the interest of making the calculations more precise we developed an analysis based on computing variation which treats a ferrite resonator connected with one line as a discontinuity problem, reducing the error which was caused earlier by the magnetic field presumed to be a constant in the coupling plane (P. Barsony, A Method for Calculating Anistotropic Planar Circuits, Fifth International Conference on Microwave Ferrites, 1980, Vilnius, and A Method for Analysing the Constituent Resonator of Circulators, Seventh Colloquium on Microwave Communication, 1982, Budapest). This analysis, which can be done on a desktop computer, introduces effective parameters to take into consideration the effect of dispersed fields which always caused a large error earlier in the microstrip case. Using the analysis the design of microstrip circulators can be carried out with a precision of a few percentage points, which is acceptable in practice. On the basis of the model used in the analysis one can also calculate the temperature dependence of the circulators (P. Barsony, Temperature Dependence of Constituent Resonator of MIC Circulators, Eighth Colloquium on Microwave Communication, 1986, Budapest and Analysis of Temperature Dependence of MIC Circulators, Eighth International Conference on Microwave Ferrites, 1986, Ilmenau). The model studies led to the recognition that it would be possible to increase the temperature stability of circulators if we made the circuit connecting the circulator to the gates with the proper temperature dependence (P. Barsony, On Temperature Stabilization of MIC Circulators by Transformers, 1987 SBMO International Microwave Symposium, Rio de Janeiro). In the case of the most commonly used lambda/4 transformer connection this means that the transformer is formed on a ferrite substrate with a temperature dependence greater than the ferrite resonator so that with increasing temperature the characteristic impedance of the transformer increases, this happens because of the temperature dependence of the resonator part, effectively reducing the deterioration in the circulator parameters. It is possible to derive equations for the design of circulators compensated in this way (P. Barsony, Temperature Stable MIC Circulator on a Composite Substrate, MIOP 88, 1988, Wiesbaden). [passage omitted]

4. Developing Microstrip Circulators

[Passage omitted] At the TKI we based the development of microstrip circulators largely on the use of garnet substrates. In this case both the ferrite resonator and the connecting circuit are formed on the same substrate. At higher frequencies we use disk resonators and under 3 GHz we use other type resonators (triangular, etc.) when forming the circulators, in the interest of reducing size.

To achieve the prescribed band width we do the matching with one or two step transformers, keeping in view the requirement that the circuits should be realizable at the smallest possible size. With inhomogeneous magnetization of the transformer sections we were able to increase band width even when using short transformers (P. Barsony, Some Effects of Inhomogeneous Biasing Fields for MIC Circulators, Fourth International Conference on Microwave Ferrites, 1968, Jablonna). For example, one can achieve inhomogeneous magnetization by designing one magnet of the microstrip circulator with a smaller diameter and the other with a greater.

We usually use ferrite magnets—these are the most economical—but in a few cases, for example in the case of a greater temperature stability requirement, we use metal or rare earth metal magnets.

Relying on domestic materials we developed a product family which is used primarily in microwave main line network systems in the 4 GHz, 6 GHz, 7 GHz and 8 GHz frequency bands. The circulators and isolators embrace the communications bands with parameters of stop-band attenuation greater than 20 dB, pass-band attenuation less than 0.5 dB and a standing wave ratio less than 1.25.

Table 2 summarizes, without trying to be complete, the technical data characterizing the 4, 6 and 8 GHz ferrite devices.

Table 2.

Type	Frequency band in MHz	Typical data		
		A_a in dB	A_z in dB	FAHA*
MIP4V	3390-3900	0.4	23	1.17
MIP4Z	3790-4200	0.4	23	1.17
MIP6N	5600-6200	0.5	23	1.17
MIP6Q	5900-6500	0.5	23	1.17
MIP7	7100-7800	0.4	23	1.17
MIP8A1	7700-8500	0.4	24	1.17
MCP8A	7700-8500	0.4	24	1.17

[Note: "FAHA" in the table presumably stands for "specific standing wave ratio."]

We make the isolators out of circulators by terminating and connecting the third gate of the circulators with a 50 ohm resister mounted on the surface of the garnet substrate. We can make coaxial circulators and isolators* by boxing the microstrip ferrite devices and putting on SMA connectors.

We also developed small size, very broad bandwidth devices in boxed versions.

5. Development of Strip Circulators

Above 10 GHz, because of the small dimensions due to the high permittivity (a value of about 15) of microwave ferrites and other problems with the microstrip technique, it is useful to make boxed devices with the strip line technique. This generally results in lower pass-band attenuation as well. The 13 GHz ferrite device family is based on domestic Li-ferrite material and was developed in symmetrical tape feed line. The devices are basically three-gate circulators which we mount with an outside terminator for isolator purposes; for multi-gate uses we connect two three-gate circulators together. The connection of the disk resonators is done with a two-step transformer.

6. Conclusions

As a result of device development done on the basis of ferrite materials developed at the TKI the institute developed a family of modern microstrip and strip line circulators and isolators with good parameters which is suitable for use in modern third generation microwave systems.

Research at Hungarian Telecommunications Institute Reviewed

25020258a Budapest HIRADASTECHNIKA in Hungarian No 2, 1989 p 33

[Introduction to special issue by Dr Gyula Tofalvi, scientific director of the Telecommunications Research Institute (TKI)]

[Text] For months I have watched with great attention the efforts of Dr Andras Baranyi to successfully put together a special issue on the TKI which would provide an optimal sampling of the research and development and scientific life at the Telecommunications Research Institute.

He had to attempt this in a double bind.

On the one side, as a leading researcher and scientific adviser for the TKI, he had to have a spiritual and professional compulsion to show all the essential research going on now but from the other side, as leading editor of the TKI column for our scientific journal, he had to know that his available space was so limited that he himself would have to limit his aspirations.

So it was foreseeable that his struggle with limited space and ample material could be solved only by a compromise.

He knew well also that in one special issue he could give only a taste of the rich research and development work and scientific life at the Telecommunications Research Institute which includes digitalization, light telecommunications, space telecommunications, use of new frequency ranges, increasing signal transmission speeds, modern solutions for rural telecommunications, etc. along with analysis of many themes representing basic research and coordination of multi-national technical-scientific tasks.

To see how difficult this search for a compromise could be in the telecommunications theme alone it is enough to note that in this special issue there was no room for the research and development now being conducted in regard to the 140 Mbps, 6 GHz microwave equipment, further development of the INTERCSAT equipment, digital light transmission, devices for digital signal transmission, etc.

Going beyond the research developments mentioned it would have been good to report briefly on or exchange ideas concerning:

—the present achievements and problems of the more than 25 years of TKI-NIIR [Radio Industry Research Institute, Moscow] cooperation,

—preparations for the joint scientific meeting EUROPEAN MICROWAVE CONFERENCE-MICROCOLL to be held in Budapest in 1990,

—the experiences with or lessons of research and development connected with OKKFT-A/5 and OKKFT-G/1 [programs of the National Medium-Range Research and Development Plan] and TELECOM'87,

—the status and future of industrial research in Hungary,

—the international dimensioning of the Hungarian telecommunications industry, etc.

I could go on that in my opinion the readers of our journal would like to hear from those scientists, researchers and developers who, with their scientific foundation in creative work, are capable of reviewing the scientific-professional essence of individual research and development tasks and thus the probable future of the Hungarian electronics industry and of the Hungarian telecommunications industry therein.

I must confess that if I had received Dr Andras Baranyi's task I would not have been able to reach a better compromise under the given conditions than is provided by the special TKI issue now being published.

So what can we promise after all this?

We will continue this reporting in subsequent issues of HIRADASTECHNIKA because it is a pleasure not only to research, develop and create but also to show our achievements and ideas to the surrounding world.

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